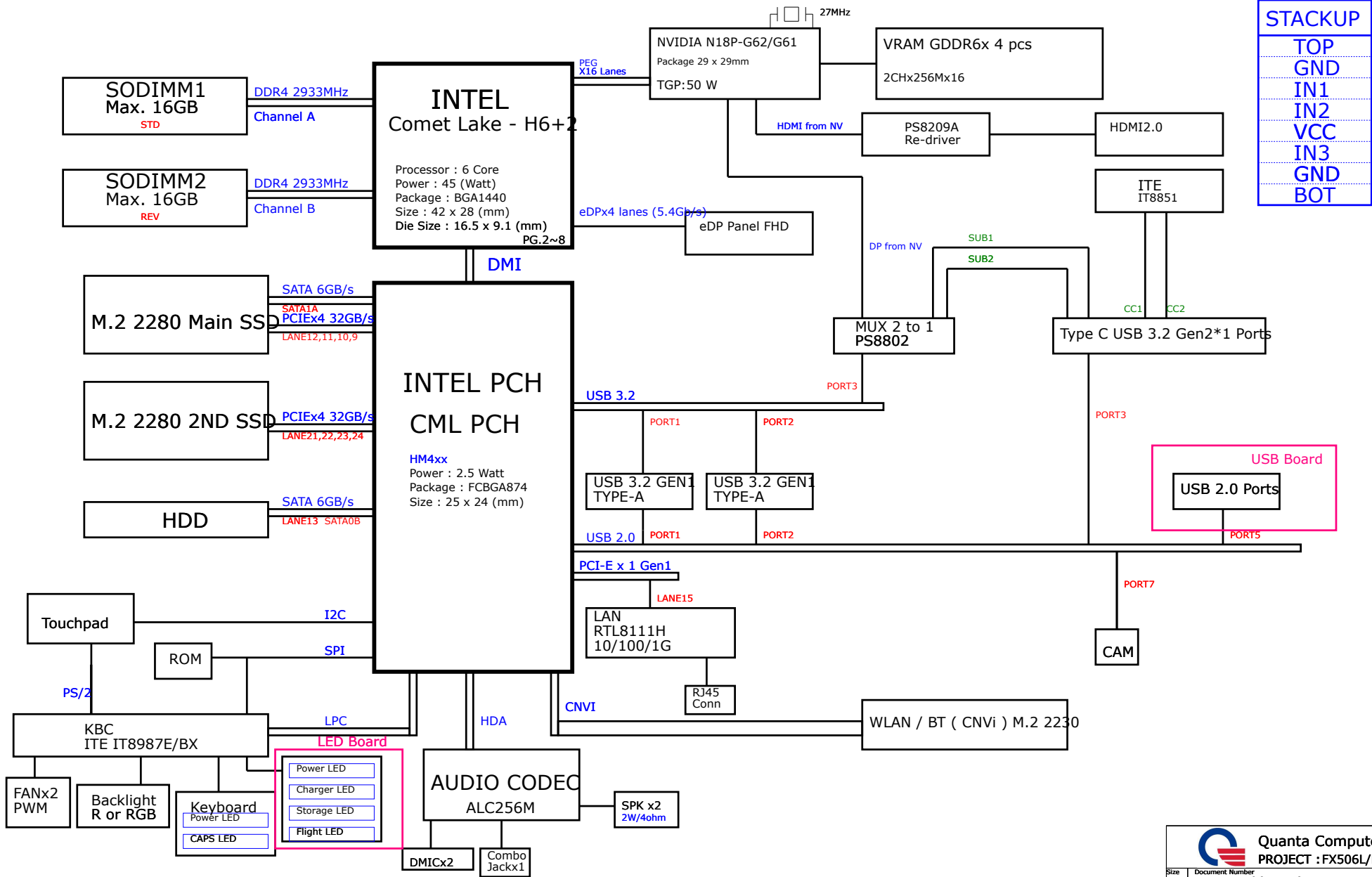


ASUS FX506LI/FX506LH/FX706LI N18P-G62/G61 Block Diagram

01



Model
FX506LT
FX706LT

REV

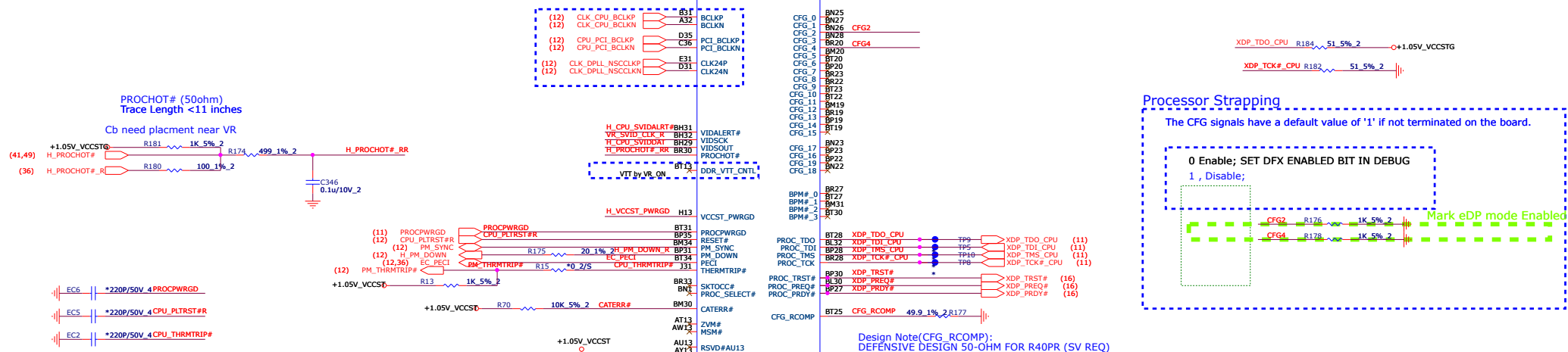
CHANGE LIST

Item	Stage	Page	Owner	Change explanation
01	ER	29	EE	ER-E00:Del RUN_ON for 1.2V_MUX enable....1113
02	ER	29	EE	ER-E01:Change G9090 to G9661 to solve PD issue.and +1.2V_HDMI ripple issue....1113
03	ER	29	EE	ER-E02:Add N-MOSFET to +1.2V_HDMI for ripple issue....1113
04	ER	39	EE	ER-E04:Change +1.2V to +1.2V_HDMI power rail name....1113
05	ER	29	EE	ER-E05:Del +3V power rail and SR9 and SR7 to shortpad....1113.
06	ER	29	EE	ER-E06:Change +3V_PD to LDO for ripple issue....1113.
07	ER	39	EE	ER-E07:ADD DISCHARGE FOR to +1.2V_HDMI power rail name....1113
08	ER	29	EE	ER-E08: No mount SR82 for surge issue....1113.
09	ER	29	EE	ER-E09:DEL PD to MUX_SMBUS....1113
10	ER	29	EE	ER-E10:Change no mount:SQ1,SR66,SR67, NO USED....1113.
11	ER	39	EE	ER-E11:Change no mount:HQ3, NO USED....1113.
12	ER	29	EE	ER-E12:Change SR61,SR62,SR63 TO NO-MOUNT for shortpad....1113.
13	ER	11	EE	ER-E13:Change R206 TO NO-MOUNT for shortpad....1113.
14	ER	16	EE	ER-E14:Change R858 and C1094,R856 TO NO-MOUNT....1113.
15	ER	7	EE	ER-E15:Change C269 1000P to 10U_4 for power ripple....1113.
16	ER	18	EE	ER-E16:Add 0.1u near MR5....1113
17	ER	19	EE	ER-E17:Add 0.1u near MR10....1113.
18	ER	32	EE	ER-E18:Change C1116 *470 to 10U_4 for ripple....1113.
19	ER	22	EE	ER-E19:Change GPIO27_IPFC_HPD to GPIO27_IPFC_HPD# for Low active....1113.
20	ER	22	EE	ER-E20:Change GPIO18_IPFE_HPD to GPIO18_IPFE_HPD# for Low active....1113.
21	ER	28	EE	ER-E21:Del RP1/RP2/RP3/RP4 and EMI by pass for EMI request....1113.
22	ER	07	EE	ER-E22:Change C289,C73,C72 From 47uF to 22uF for PASS VRTT....1119
23	ER	29	EE	ER-E23:Change SU10 part number for E ver and 08FW to fix PD.0 fail issue....1120.
24	ER	36	EE	ER-E24:Change KR122 0ohm to no-mount for no support....1120
25	ER	28	EE	ER-E25:Change EMIL5,EMIL6 to BLM15AG221SN1D and C1072 C1073 to 10P for EMI issue and signal pass....1122.
26	ER	31	EE	ER-E26: Change 2.1ohm to 5.1ohm for fix TDR issue....1122.
27	ER	12	EE	ER-E27: Change R43 to no-mount and add R874 100K to GND for fixed GPU timing issue....1122.
28	ER	23	EE	ER-E28: Change VR113 to 10Kfor fixed GPU timing issue....1122.
29	ER	34	EE	ER-E29: Change C355,C356 to no-mount for fix TP timing issue....1122.
30	ER	35	EE	ER-E30:Add AR47 moat resistor between AGND&DND and connect to AU1 pin20 for active speaker noise issue in SS....1122.
31	ER	37	EE	ER-E31:Del KQ15/KQ13 for no support Red backlight....1125.
32	ER	53	Power	ER-001:PR358 from 100ohm to 105ohm for +1.0V_GPU output voltage.
33	ER	48	Power	ER-002:Add PC169 & PC170 47pF for ASUS'SOW.
34	ER	41	Power	ER-003:Change PR1093 from 16.9K to 1.87K to set IA iccmax 128A for CMH base.
35	ER	41	Power	ER-004:Change PC1061 from 68pF to 330pF to correct L_DCR matching.
36	ER	41	Power	ER-005:Change PR1078 from 422 to 412 ohm to to set OCP 180A for H62.
37	ER	41	Power	ER-006:Change PC1068 from NI to 47nF to correct L-CDR matching.
38	ER	41	Power	ER-007:Change PR1057 from 107K to 113K to correct IMONA for H62.
39	ER	41	Power	ER-008:Change PR1078 from 365 to 287 ohm to set OCP 116A for H42.
40	ER	41	Power	ER-009:Change PR1057 to 76.8K to correct IMONA for H42.
41	ER	41	Power	ER-010:Change PR1070 from 5.11k to 3.48k to correct DCLL for H42.
42	ER	43	Power	ER-011:PC1333,PC1334,PC1335,PC1336,PC1337,PC1338 add 22uF to pass Intel 20mV Ripple voltage at PS0 , original 25mV Ripple failure Intel Ripple voltage spec for H62/H42 GT.
43	ER	41	Power	ER-012:Change PC1044 from 10nF to 15nF to correct L_DCR matching for H62/H42 SA.
44	ER	41	Power	ER-013:Change PC1050 from 220pF to 680pF to reduce undershoot for H62/H42 SA.
45	ER	47	Power	ER-014:Delete PD13 & PD14 for SHDN# issue.
46	ER	47	Power	ER-015:PC157 1000P change to 2200P for meet HDD rise time SPEC.
47	ER	47	Power	ER-016:PC164 1000P change to 680P for meet TP rise time SPEC.
48	ER	45	Power	ER-017:PR642 change to 6.49K+-1% for output voltage up.
49	ER	49	Power	ER-018:PD11 & PQ40 change mount & PR240 change no-mount for ADP plug-out issue.
50	ER	41~55	Power	ER-019:0ohm change to short pad.
51	ER	44~53	Power	ER-020:Remove output short pad.
52	ER	45	Power	ER-021:PU1327 all component change to non-mount & +1.05V_VCCSTG source change to PU32 side for EE request.
53	ER	35	EE	ER-E31:AR14 and AR5 change from 22 ohm to 10 ohm increasing the FSOV margin.
54	ER	30	EE	ER-E32:Remove CON6 for USB board FFC CONN
55	ER	47~49	Power	ER-022:Add test point PTP1~PTP6 for ASUS' request.
56	ER	47	Power	ER-023:Reserve PEC51 0.1uF for EMI request.
57	ER	30	EE	ER-E33:Reserve CON6 for USB board FFC CONN
58	ER	31	EE	ER-E34:KR64, KR65, KR66, KR67, KR68 change from 390 to 931 ohm for brightness
59	ER	49	Power	ER-024:PR238 change to 0ohm & PR232 change to 16Kohm for Psys Pmax setting.
60	ER	16	EE	ER-E35:Reserve U28 for C10 GATE# support.
61	ER	48	Power	ER-025:PCN1 change to DFHD06MR208 for Blistering issue, so the manufacturer changed the material from PA6T CHANGE TO LCP.
62	ER	35	EE	ER-E36:AL5,AL5 change to C16011 2000I and AR14,AR15 change to 22 ohm for FSOV
63	ER	17	EE	ER-E37:Add EMIC87,EMIC88 for RF
64	ER	29	EE	ER-E38:SU12 change from SY6863B3ABC to G518B1TP1U, SR55 change to 18.7K, SR54 change to 8.87K for ILIM.
01	PR	35	EE	PR-E01:ACN1 Change PIN Define
02	PR	30	EE	PR-E02:Remove CON6 for USB board FFC CONN
03	PR	29	EE	PR-E03:Mount SU15 for DP HPD
04	PR	14	EE	PR-E04:Add BOARD ID0 define for I7&I5
05	PR	17	EE	PR-E05:Add EMC89/EMC91/EMC93 0.1uF and EMC90/EMC92/EMC94 for EMI, EMC89 and EMC90 un-mount for Height limitation
06	PR	30	EE	PR-E06:L8/L9/L12/L13 change to RFL11T2SA0AR for RF
07	PR	17	EE	PR-E07:EMIC35/EMIC57/EMIC38/EMIC42 change from 100p to 2200p, EMIC37/EMIC47/EMIC40 change from 100p to 0.1u for EMI
08	PR	39	EE	PR-E08:HDMI DDC pull-up resistor HR20/HR21 change from 2.2K to 3K for HDMI protocol issue
09	PR	48	Power	PR-001:Add PEC27 0.1uF for EMI request.
10	PR	49	Power	PR-002:Add PEC28 2200pF for EMI request.
11	PR	47/11	EE	PR-E09:mount R190, R193, R12 and remove R872, R873 for HDMI lag issue
11	PR	37	EE	PR-E10:KR84, KR86 change from 220 ohm to 2.2K ohm for ID KB LED brightness request.

DOC NO.	PROJECT MODEL : BKLG/BKLN	APPROVED BY:	DATE: 2018/01/17
	PART NUMBER:	DRAWING BY:	REVISION: 1A

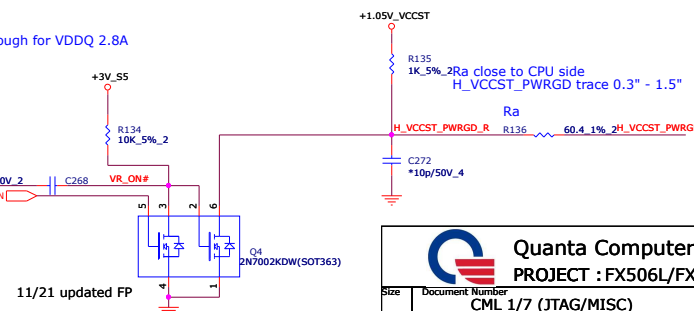
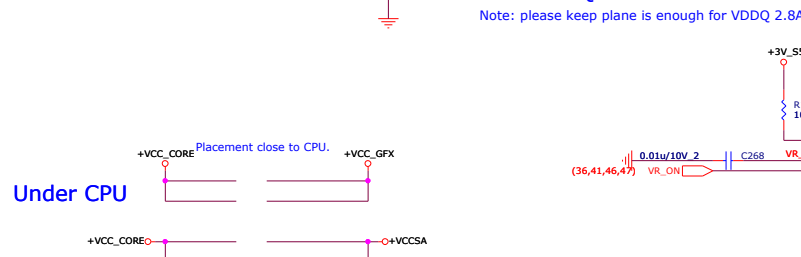
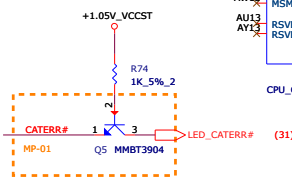
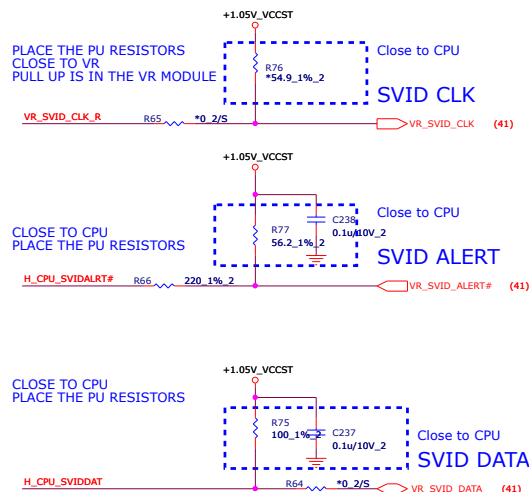
Comet Lake Processor (CLK,MISC,JTAG)

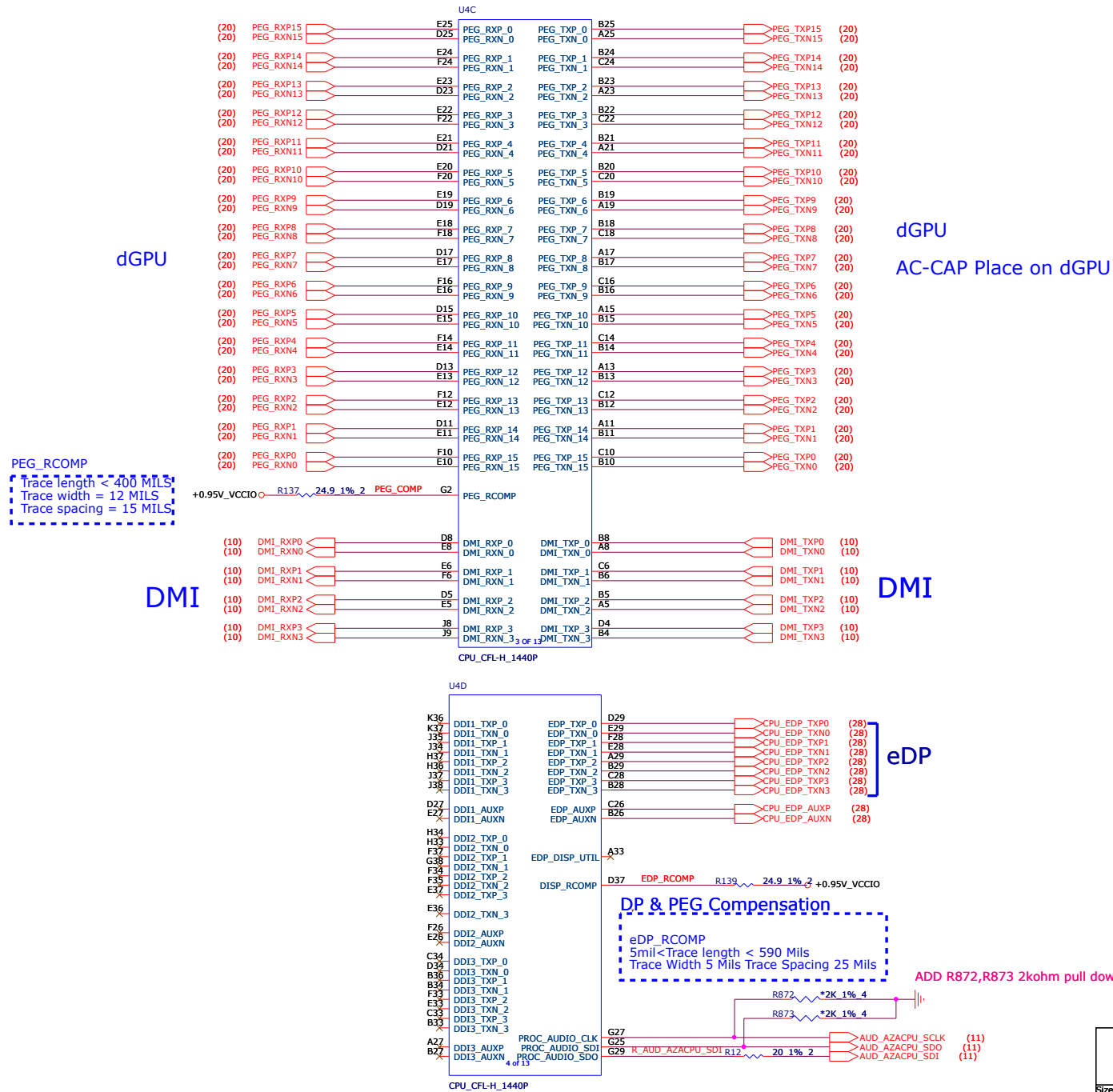
Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impedence 85 ohm^{4E}



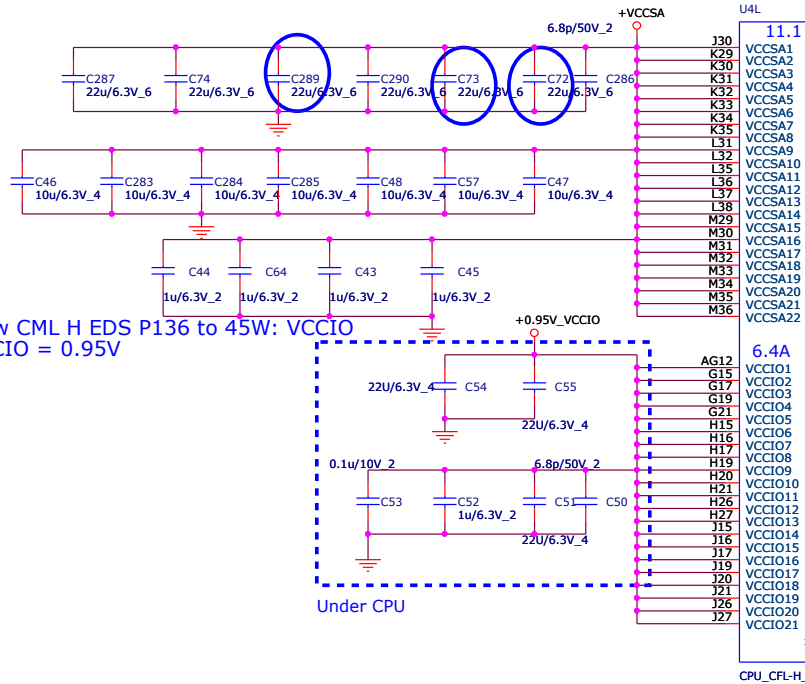
CPU CORE SVID

Layout note:
1. Need routing together
2. ALERT need between CLK and DATA.

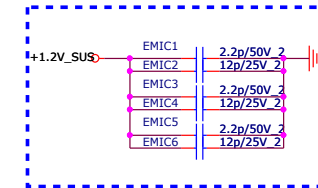
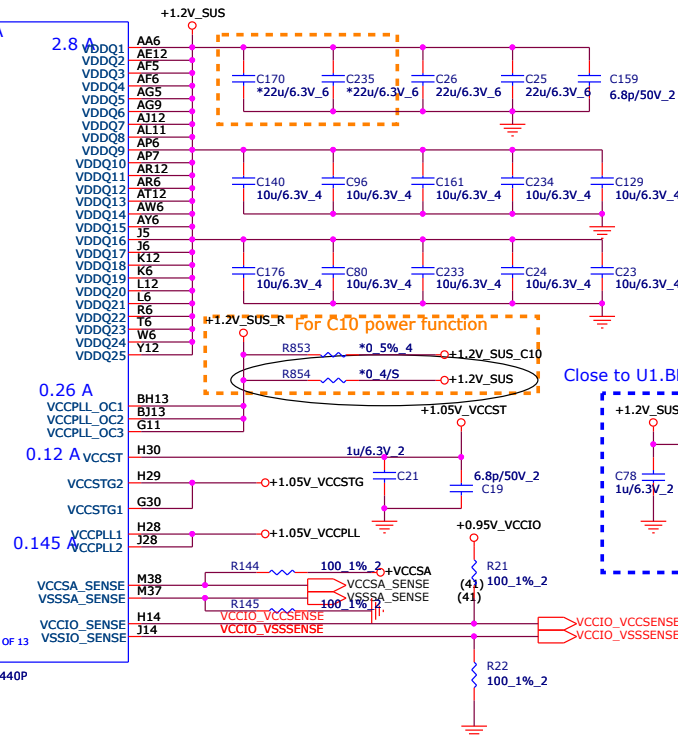




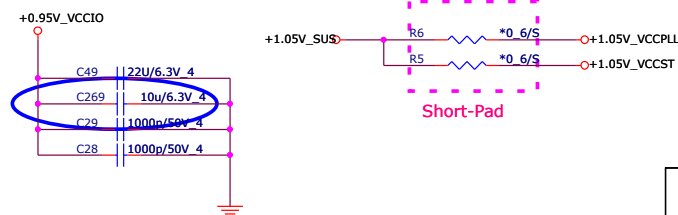
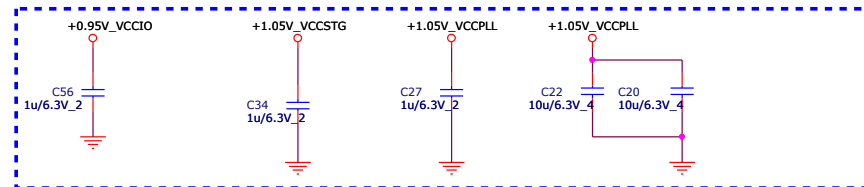
Follow CML H EDS page 135 to 45W(GT2): VCCSA=11.1A
ER-022:Change C289,C73,C72 From 47uF to 22uF for PASS VRTT...1119



Follow CML H EDS page 135 45W: VDDQ=3.3A



Close CPU

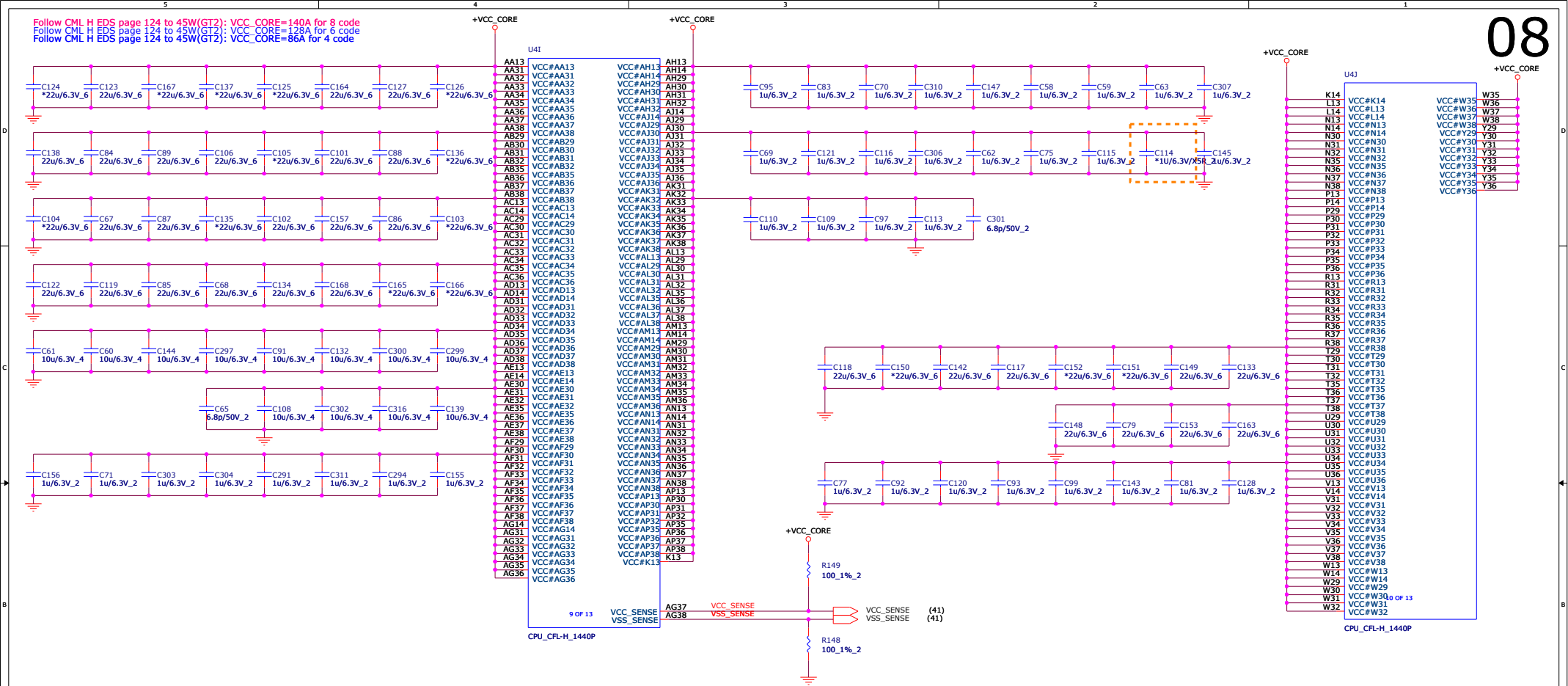


ER-015:Change C269 1000P to 10U_4 for power ripple....1113.



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PROJECT : FX506L/FX706L

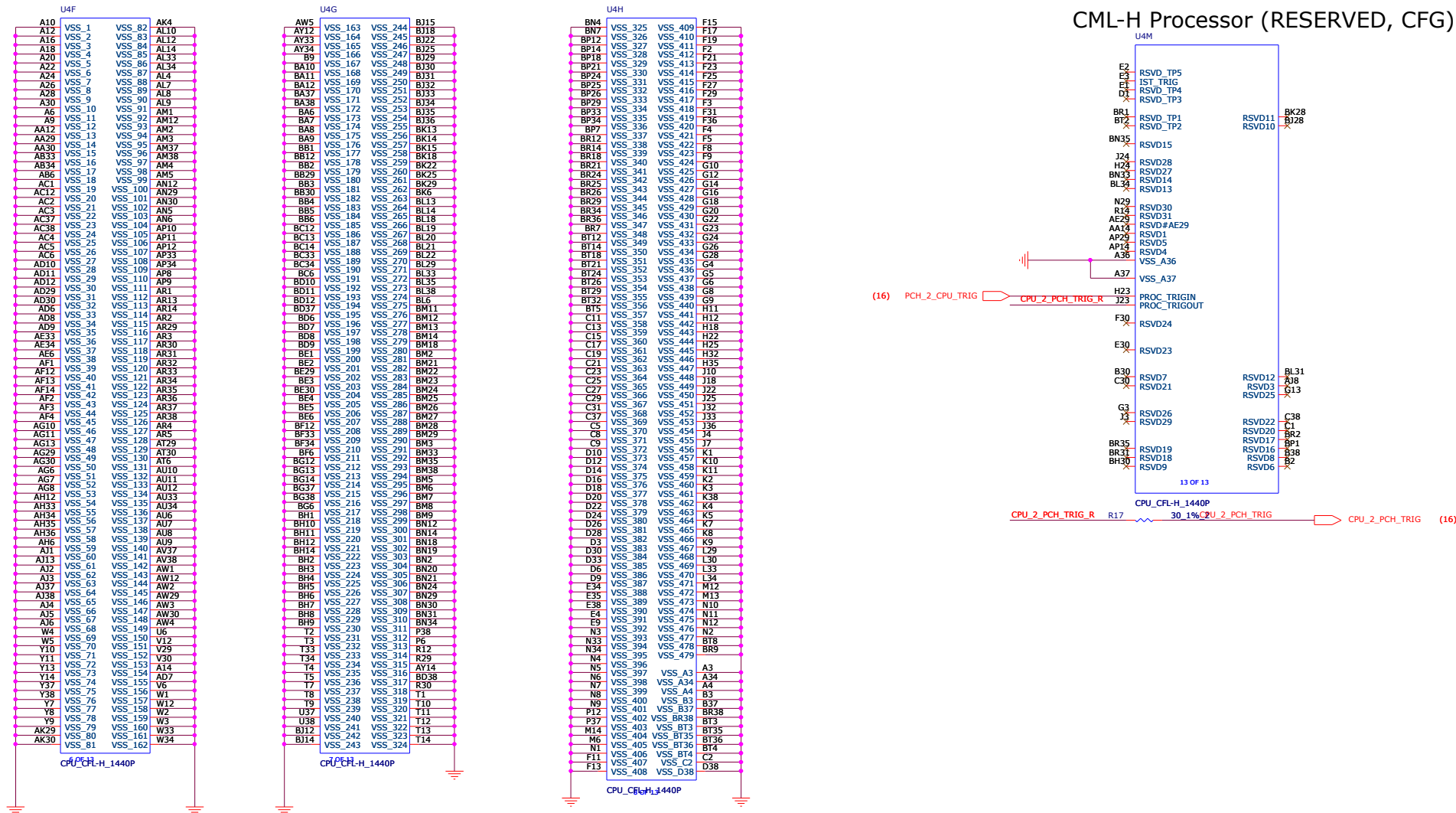
Follow CML H EDS page 124 to 45W(GT2): VCC_CORE=140A for 8 code
 Follow CML H EDS page 124 to 45W(GT2): VCC_CORE=128A for 6 code
 Follow CML H EDS page 124 to 45W(GT2): VCC_CORE=86A for 4 code



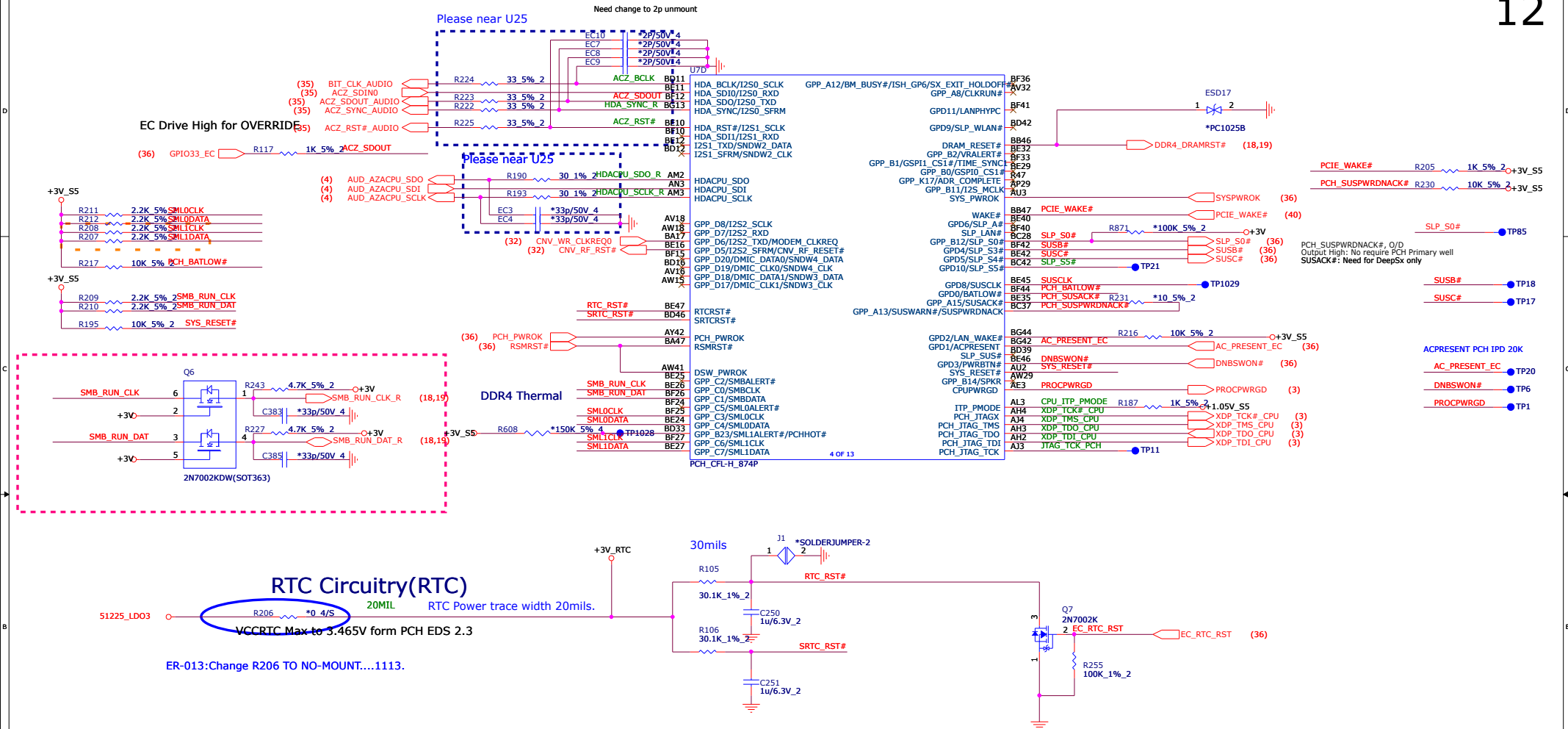
Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket
 Trace Impedance 50 ohm

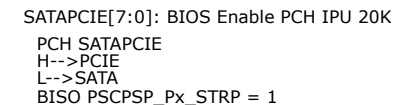
CML-H Processor (GND)

CML-H Processor (RESERVED, CFG)







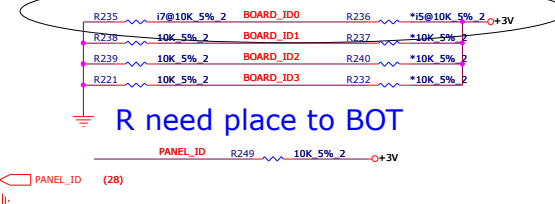


The diagram illustrates the i.MX8M Mini board's internal connections. Key components and their connections include:

- Power and Clock Inputs:**
 - 3.3V and 5V power rails connected to various pins.
 - 24MHz/10p/30ppm crystal (Y1) connected to XTAL24_IN_PCH and XTAL24_OUT_PCH.
 - 32.768KHz/12.5p/20ppm crystal (Y2) connected to RTC_X1 and RTC_X2.
- Peripheral Connections:**
 - CPU:** Connections for CPU_PCI_BCLKN, CPU_PCI_BCLKP, and CNV_384_CLK.
 - GPU:** Connections for CLK_PCIE_GLANN, CLK_PCIE_GLANP, CLK_PCIE_VGA_N, and CLK_PCIE_VGA_P.
 - SSD:** Connections for CLK_PCIE_SSDN, CLK_PCIE_SSDP, CLK_PCIE_SSD2N, and CLK_PCIE_SSD2P.
- Processor Pin Connections:**
 - XTAL24_IN_PCH and XTAL24_OUT_PCH connected to XTAL24_IN and XTAL24_OUT.
 - RTC_X1 and RTC_X2 connected to RTC_X1 and RTC_X2.
 - Various other pins connected to the processor's internal components.

The diagram is a detailed representation of the board's internal wiring, showing the connection of various components to the processor pins. The components are color-coded to match the image, and the connections are labeled with their respective pin numbers and component values.



[illegible]

This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.

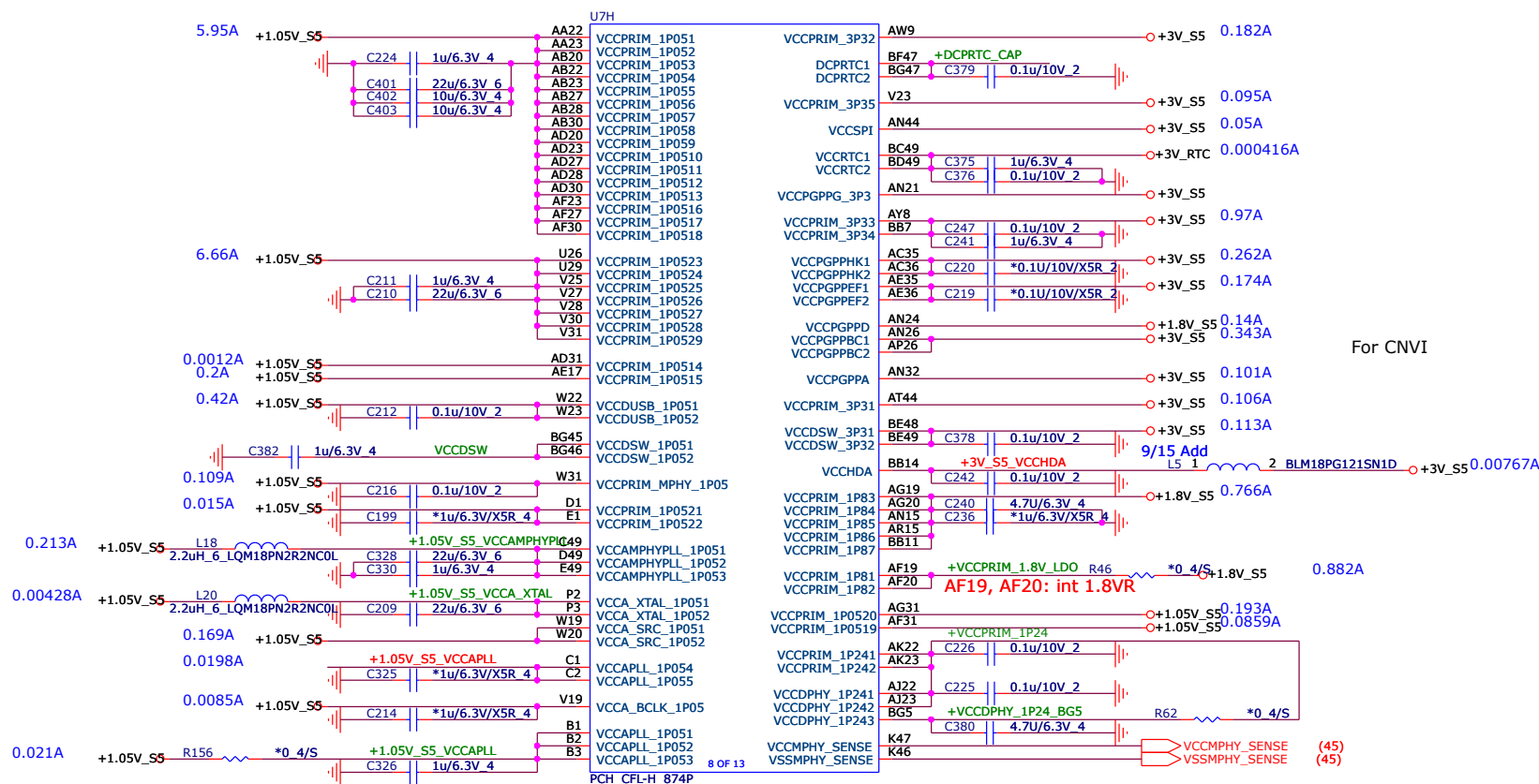
Pin Name	Strap description	Sampled	Configuration	xxx PCH STRAPS SETTING STATUS
GPP_B14 (SPKR)	Top Swap Override	PCH_PWROK	0 = *Disable Top Swap (IPD 20K) Default 1 = Enable Top Swap Mode	
GPP_B18 (GSP10_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (IPD 20K) Default 1 = Enable No Reboot Mode	
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSRMRST#	0 = *Disable Intel ME Crypt to TLS(IPD 20K) Default 1 = Enable Intel ME Crypt to TLS to support AMT TLS	
GPP_B22 (GSP11_MOSI)	Boot BIOS Strap Bit BBS	PCH_PWROK	0 = *SPI (IPD 20K) Default 1 = LPC	
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSRMRST#	0 = *LPC is selected for EC (IPD 20K) Default 1 = eSPI selected for EC	
SPI0_MOSI	Reserved	RSRMRST#	(IPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
GPP_H15 (SML3ALERT#)	Reserved	RSRMRST#	(IPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSRMRST#	(IPD 20K) This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
SPI0_IO2	Reserved	RSRMRST#	(IPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
SPI0_IO3	Reserved	RSRMRST#	(IPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
HDA_SDO (I2S0_TXD)	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (IPD 20K) Default 1 = Disable Flash Descriptor Security (Override)	EC Drive High for OVERRIDE
GPP_H12 (SML2ALERT#)	eSPI Flash Sharing Mode	RSRMRST#	0 = *Master Attached Flash Sharing (MAFS) enabled (IPD 20K)Default 1 = Slave Attached Flash Sharing (SAFS) enabled.	
GPP_I6 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (IPD 20K) (Default) 1 =Port B is detected	
GPP_I8 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (IPD 20K) (Default) 1 =Port C is detected	
GPP_I10 (DDPD_CTRLDATA)	Display Port D Detected	PCH_PWROK	0 = *Port D is not detected (IPD 20K) (Default) 1 =Port D is detected	
GPP_F23	Display Port F Detected	PCH_PWROK	0 = *Port F is not detected (IPD 20K) (Default) 1 =Port F is detected	CFL - H CPU Not Support DDI Port F
GPP_J4 CNV_BRI_DT/UART0_RTS#	XTAL Frequency Select	RSRMRST#	An external pull-up is required on this strap since 38.4MHz XTAL is not supported on the PCH. 0 = *38.4MHz XTAL frequency selected. (IPD 20K) (Default) 1 = 24MHz XTAL frequency selected.	
GPP_J6 CNV_RGI_DT/UART0_TXD	M.2 CNV Mode Select	RSRMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. (Default) 1 = Integrated CNVi disable.	
GPP_J9	1.8V VCCPSPI	RSRMRST#	0 = *VCCPSPI is connected to 3.3V rail. (IPD 20K) (Default) 1 = VCCPSPI is connected to 1.8V rail	
GPD7	Reserved	DSW_PWROK	This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	External pull-up is required. Recommend 100K.

Change R58,R59,R843,R842 mount to no mount for no support DDI....Tommy_0903

PCH Strap: GPP_J6 = M.2 CNVI STRAP
HIGH -> DISABLE / LOW -> ENABLE

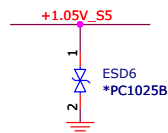
Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

need to add +1.05V power rail

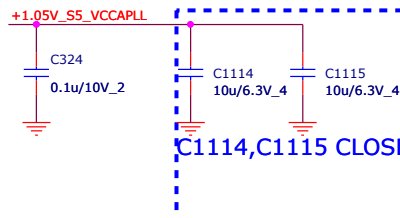


For CNVI

ESD6 CLOSE TO U7



C324 CLOSE TO U7.B2



- 1.24V for CNVi logic = VCCDPHY_1P24 & +VCCPRIM_1P24
- This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC.

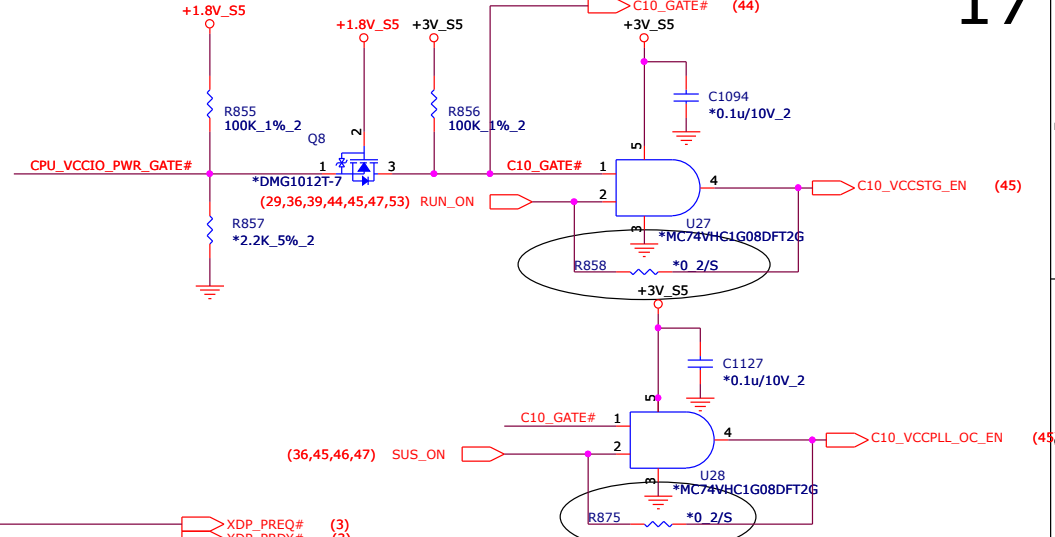
Refer to the Platform Design Guide for implementation details.



Quanta Computer Inc.
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Size	Document Number	Rev
	PCH 6/7 (POWER)	2A
Date:	Tuesday, March 24, 2020	Sheet 15 of 59

ER-014:Change R858 and C1094,R856 TO NO-MOUNT.....1113.



ER-E35:Reserve U28 for C10 GATE# support.

U7L

BG3	VSS_145	VSS_196	M24
BG33	VSS_146	VSS_197	M32
BG37	VSS_147	VSS_198	M34
BG4	VSS_148	VSS_199	M49
BG48	VSS_149	VSS_200	M5
C12	VSS_150	VSS_201	N12
C25	VSS_151	VSS_202	N16
C30	VSS_152	VSS_203	N34
C4	VSS_153	VSS_204	N35
C48	VSS_154	VSS_205	N37
C5	VSS_155	VSS_206	N38
D12	VSS_156	VSS_207	P26
D16	VSS_157	VSS_208	P29
D17	VSS_158	VSS_209	P4
D30	VSS_159	VSS_210	P46
D33	VSS_160	VSS_211	R12
D8	VSS_161	VSS_212	R16
E10	VSS_162	VSS_213	R26
E13	VSS_163	VSS_214	R29
E15	VSS_164	VSS_215	R3
E17	VSS_165	VSS_216	R34
E19	VSS_166	VSS_217	R38
E22	VSS_167	VSS_218	R4
E24	VSS_168	VSS_219	T17
E26	VSS_169	VSS_220	T18
E31	VSS_170	VSS_221	T32
E33	VSS_171	VSS_222	T4
E35	VSS_172	VSS_223	T5
E40	VSS_173	VSS_224	T7
E42	VSS_174	VSS_225	U12
E8	VSS_175	VSS_226	U15
F41	VSS_176	VSS_227	U17
F43	VSS_177	VSS_228	U21
F47	VSS_178	VSS_229	U24
G44	VSS_179	VSS_230	U33
H6	VSS_180	VSS_231	U38
J10	VSS_181	VSS_232	V20
J26	VSS_182	VSS_233	V22
J29	VSS_183	VSS_234	V4
J4	VSS_184	VSS_235	V46
J40	VSS_185	VSS_236	W25
J46	VSS_186	VSS_237	W27
J47	VSS_187	VSS_238	W28
J48	VSS_188	VSS_239	W30
J9	VSS_189	VSS_240	Y10
K11	VSS_190	VSS_241	Y12
K39	VSS_191	VSS_242	Y17
M16	VSS_192	VSS_243	Y33
M18	VSS_193	VSS_244	Y38
M21	VSS_194	VSS_245	Y9
	VSS_195	VSS_246	

12 OF 13
PCH_CFL-H_874P

U7I

A2	VSS_1	VSS_73	AL12
A28	VSS_2	VSS_74	AL17
A3	VSS_3	VSS_75	AL21
A33	VSS_4	VSS_76	AL24
A37	VSS_5	VSS_77	AL26
A4	VSS_6	VSS_78	AL29
A45	VSS_7	VSS_79	AL33
A46	VSS_8	VSS_80	AM1
A47	VSS_9	VSS_81	AM18
A48	VSS_10	VSS_82	AM32
A5	VSS_11	VSS_83	AM49
A8	VSS_12	VSS_84	AN12
AA19	VSS_13	VSS_85	AN16
AA20	VSS_14	VSS_86	AN34
AA25	VSS_15	VSS_87	AN38
AA27	VSS_16	VSS_88	AP4
AA28	VSS_17	VSS_89	AP46
AA30	VSS_18	VSS_90	AR12
AA31	VSS_19	VSS_91	AR16
AA49	VSS_20	VSS_92	AR34
AB19	VSS_21	VSS_93	AR38
AB25	VSS_22	VSS_94	AT1
AB31	VSS_23	VSS_95	AT16
AC12	VSS_24	VSS_96	AT18
AC17	VSS_25	VSS_97	AT21
AC17	VSS_26	VSS_98	AT24
AC33	VSS_27	VSS_99	AT26
AC38	VSS_28	VSS_100	AT29
AC4	VSS_29	VSS_101	AT32
AC46	VSS_30	VSS_102	AT34
AD19	VSS_31	VSS_103	AT45
AD2	VSS_32	VSS_104	AV11
AD22	VSS_33	VSS_105	AV39
AD25	VSS_34	VSS_106	AW10
AD49	VSS_35	VSS_107	AW4
AE12	VSS_36	VSS_108	AW40
AE33	VSS_37	VSS_109	AW46
AE38	VSS_38	VSS_110	B47
AE4	VSS_39	VSS_111	B48
AE46	VSS_40	VSS_112	B49
AF25	VSS_41	VSS_113	BA12
AF22	VSS_42	VSS_114	BA14
AF28	VSS_43	VSS_115	BA44
AG1	VSS_44	VSS_116	BA5
AG22	VSS_45	VSS_117	BA6
AG23	VSS_46	VSS_118	BB41
AG25	VSS_47	VSS_119	BB43
AG27	VSS_48	VSS_120	BB9
AG27	VSS_49	VSS_121	BC10
AG28	VSS_50	VSS_122	BC13
AG30	VSS_51	VSS_123	BC15
AG49	VSS_52	VSS_124	BC19
AH12	VSS_53	VSS_125	BC24
AH17	VSS_54	VSS_126	BC26
AH33	VSS_55	VSS_127	BC31
AH38	VSS_56	VSS_128	BC35
AJ19	VSS_57	VSS_129	BC40
AJ20	VSS_58	VSS_130	BC45
AJ25	VSS_59	VSS_131	BC8
AJ27	VSS_60	VSS_132	BD43
AJ28	VSS_61	VSS_133	BE44
AJ30	VSS_62	VSS_134	BF1
AJ31	VSS_63	VSS_135	BF2
AK19	VSS_64	VSS_136	BF3
AK20	VSS_65	VSS_137	BF48
AK22	VSS_66	VSS_138	BF49
AK27	VSS_67	VSS_139	BF72
AK28	VSS_68	VSS_140	BF73
AK30	VSS_69	VSS_141	BG22
AK31	VSS_70	VSS_142	BG25
AK4	VSS_71	VSS_143	BG28
AK46	VSS_72	VSS_144	

PCH_CFL-H_874P

CNV_RBI_DT
CNV_RBI_RSP
CNV_RGI_DT
CNV_RGI_RSP

CNV_BRI_RSP : Model Internal Pull-Up 20k
CNV_RGI_RSP : Model Internal Pull-Up 20k.
Close to U25


Follow #571483 CFL-H CRB0.9 Reserve Pull-H Resistor.



U7M

AW13	GPP_G0/SD_CMD	CNV_WR_CLKN	BE3	CNV_WR_CLKP	(32)
BE9	GPP_G1/SD_D0	CNV_WR_CLKP	BE3	CNV_WR_CLKP	(32)
BF8	GPP_G2/SD_D1	CNV_WR_D0N	BB3	CNV_WR_D0N	(32)
BF9	GPP_G3/SD_D2	CNV_WR_D0P	BB4	CNV_WR_D0P	(32)
BG8	GPP_G4/SD_D3	CNV_WR_D1N	BA3	CNV_WR_D1N	(32)
BE8	GPP_G5/SD_CD#	CNV_WR_D1P	BA2	CNV_WR_D1P	(32)
BD8	GPP_G6/SD_CLK	CNV_WT_CLKN	BC5	CNV_WT_CLKN	(32)
AV13	GPP_G7/SD_WP	CNV_WT_CLKP	BB6	CNV_WT_CLKP	(32)
AP2	GPP_I11/M2_SKT2_CFG0	CNV_WT_D0N	BE6	CNV_WT_D0N	(32)
AN4	GPP_I12/M2_SKT2_CFG1	CNV_WT_D0P	BD7	CNV_WT_D0P	(32)
AM7	GPP_I13/M2_SKT2_CFG2	CNV_WT_D1N	BG6	CNV_WT_D1N	(32)
	GPP_I14/M2_SKT2_CFG3	CNV_WT_D1P	BF6	CNV_WT_D1P	(32)
AV6	GPP_J0/CNV_PA_BLANKING	CNV_WT_RCOMP	BA1	CNV_WT_RCOMP	(32)
AR13	GPP_J1/CPU_VCCIO_PWR_GATE#	PCIE_RCOMP_N	B12	PCIE_RCOMP_N	(32)
AV7	GPP_J11/A4WP_PRESENT	PCIE_RCOMP_P	A13	PCIE_RCOMP_P	(32)
AW3	GPP_J2	SD_RCOMP_IP8	BE5	SD_RCOMP_IP8	(32)
AT10	GPP_J3	SD_RCOMP_IP3	BE4	SD_RCOMP_IP3	(32)
AY2	GPP_J4/CNV_RBI_DT_UART0_RTSB	GPPJ_RCOMP_IP81	BD1	GPPJ_RCOMP_IP81	(32)
AV4	GPP_J5/CNV_RBI_RSP_UART0_RXD	GPPJ_RCOMP_IP83	BE2	GPPJ_RCOMP_IP83	(32)
AV3	GPP_J6/CNV_RGI_DT_UART0_TXD	RSVD2	Y35	RSVD2	(32)
AW2	GPP_J7/CNV_RGI_RSP_UART0_CTS#	RSVD3	Y36	RSVD3	(32)
AU9	GPP_J8/CNV_MFUART2_RXD	RSVD#BC1	BC1	RSVD#BC1	(32)
	GPP_J9/CNV_MFUART2_TXD	TP	AL35	TP	(32)

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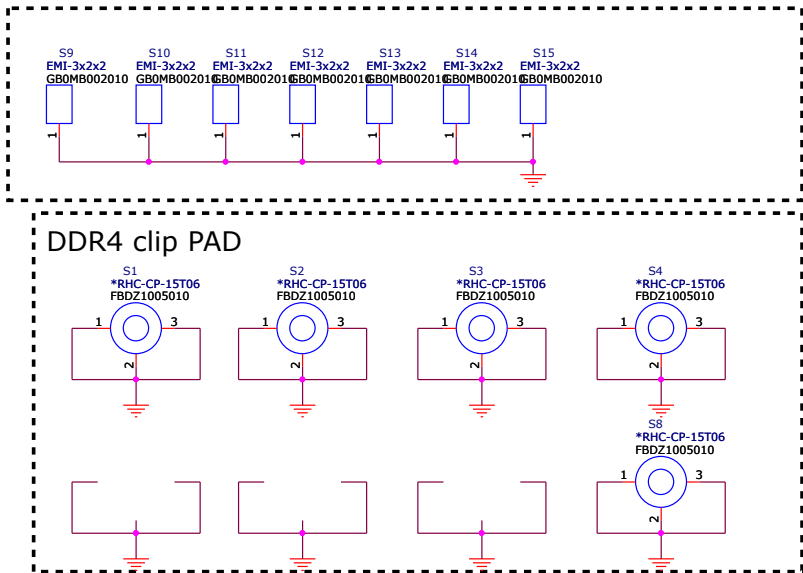


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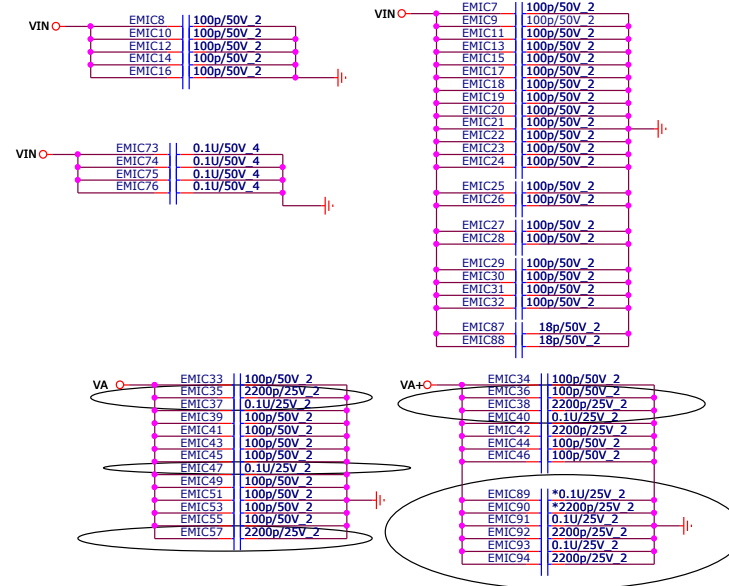
PROJECT : FX506L/FX706L

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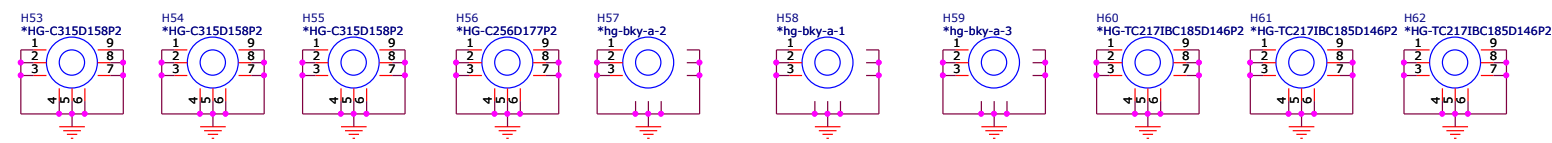
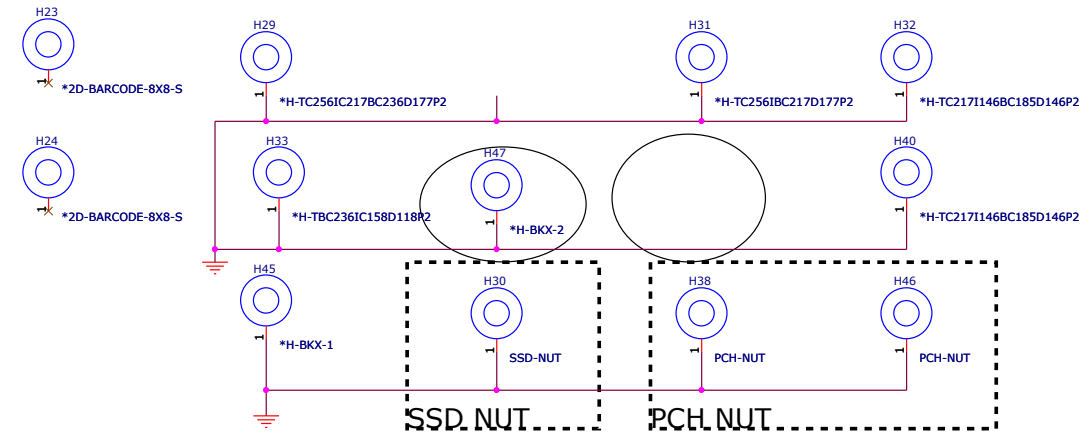
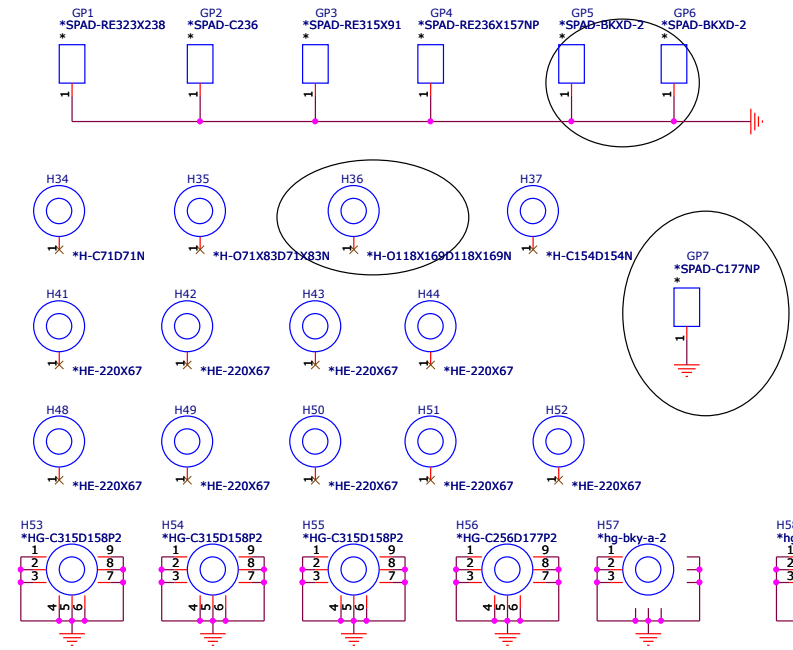
SMT GASKET-BOT

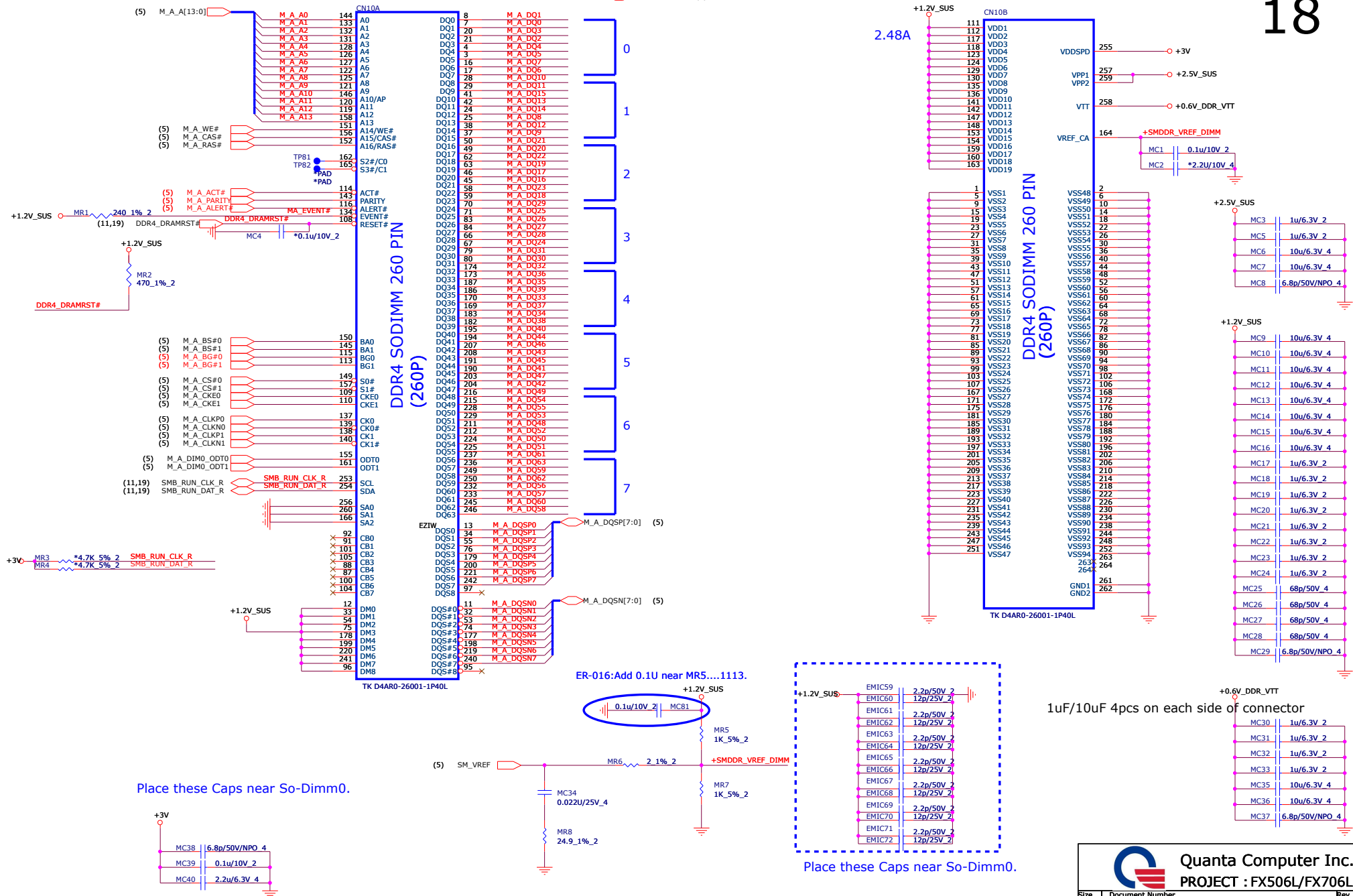


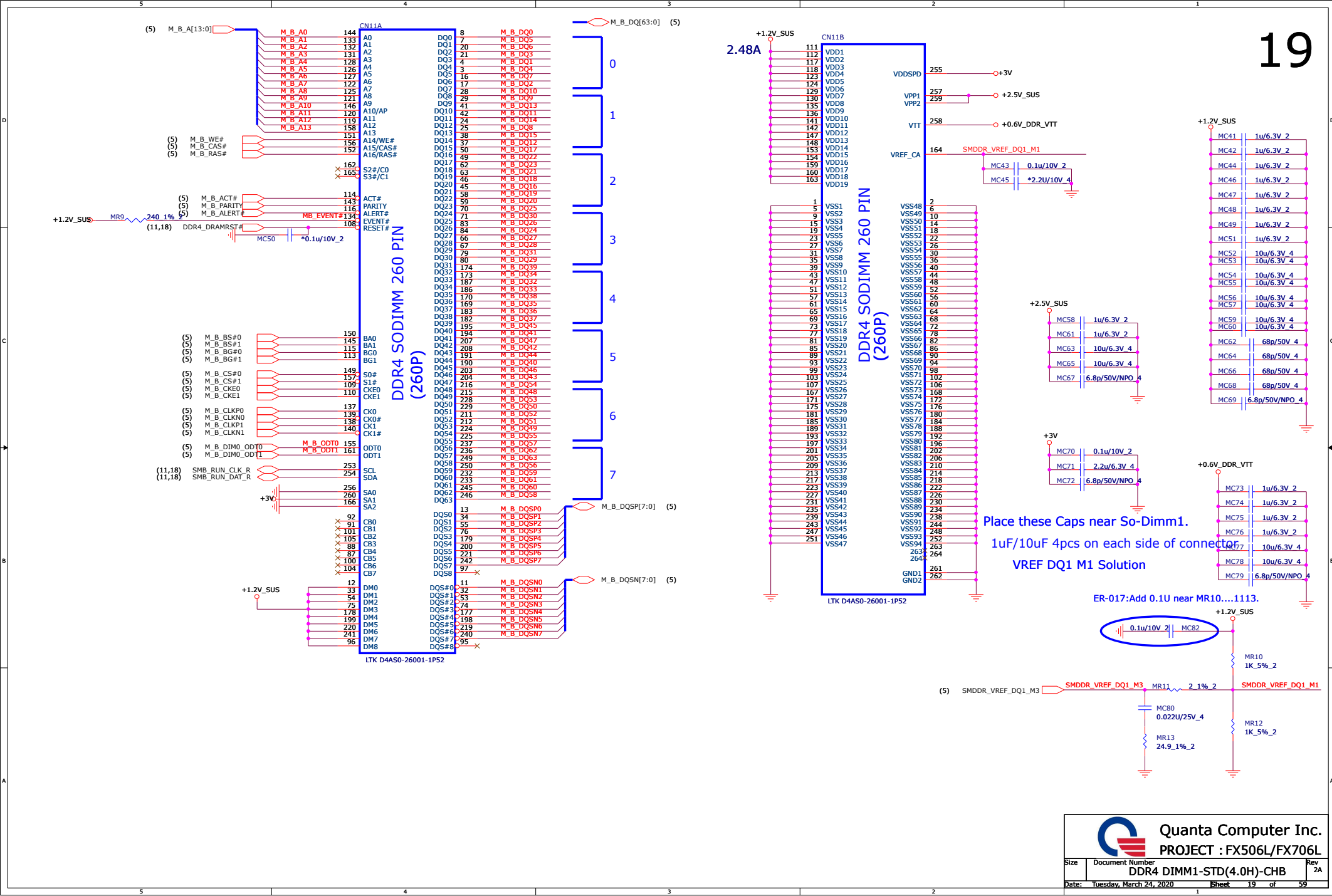
placement on TOP SIDE VIN Plane

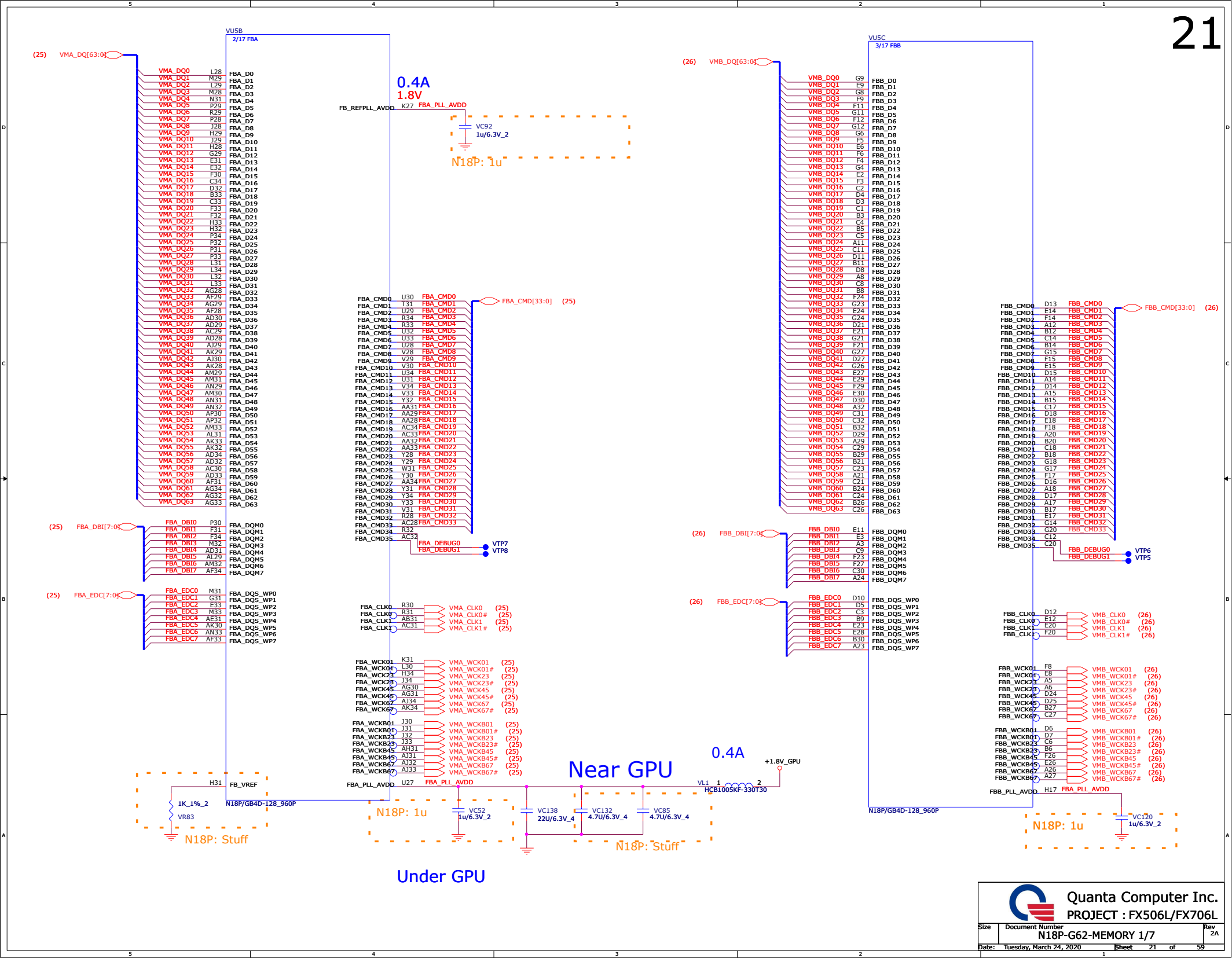


PR-E05:Add EMC89/EMC91/EMC93 0.1uF and EMC90/EMC92/EMC94 for EMI, EMC89 and EMC90 un-mount for Height limitation
PR-E07:EMIC35/EMIC57/EMIC38/EMIC42 change from 100p to 2200p, EMIC37/EMIC47/EMIC40 change from 100p to 0.1u for EMI
placement on TOP SIDE VA+ Plane

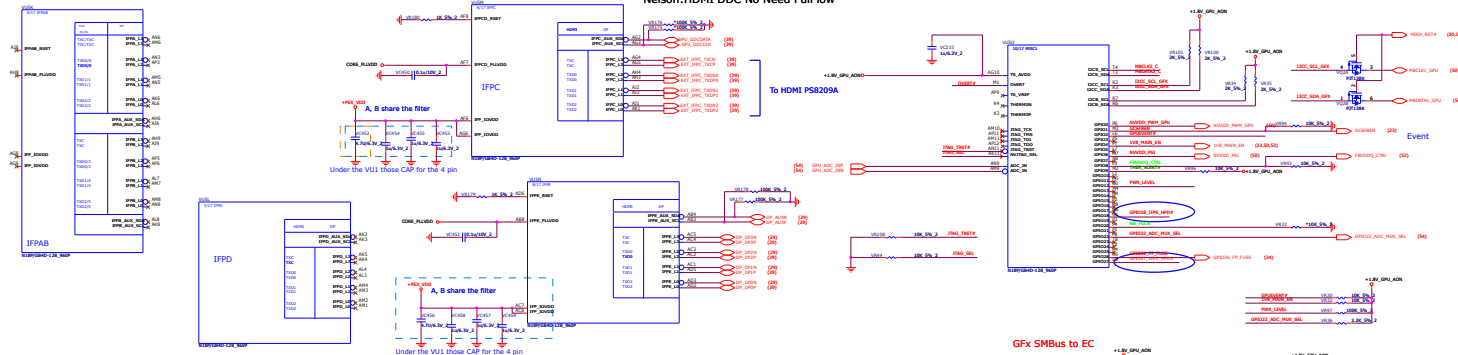








Nelson:HDMI DDC No Need Pull low



STRAP2[0] VRAM Table for N18P-G2/61 GDDR6 Recommended Memories

Device	Manufacturer	Model	Capacity	Part Number
Q1	Qimonda	Q1000 256Mx32 14 DR	1.2V	Q1000 256Mx32 14 DR
Q2	Qimonda	Q1000 256Mx32 14 DR	1.2V	Q1000 256Mx32 14 DR

Check VRAM with RVL
R need place to BOT

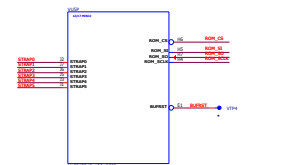
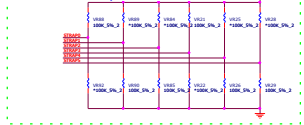
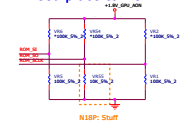


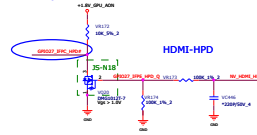
Table 5.3 RAMCFG

STRAP2	STRAP1	STRAP0	RAMCFG Setting Number
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	A	8 (0x0008)
L	L	B	9 (0x0009)
L	L	C	10 (0x000A)

R need place to BOT



ER-019:Change GPIO27_HPD_HPD to GPIO27_HPD_HPD for Low active.....1113.



ER-020:Change GPIO18_HPD_HPD to GPIO18_HPD_HPD for Low active.....1113.

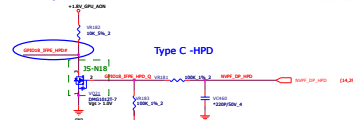


Table 14.2 GPIO Descriptions for GB4C-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	HYPER_PSR_VID	O	PSR Output to control HYPER_PSR_VID	0 to 1V8 Pull-up
GPIO1	GCMA_GCA_FR_EN	O	FR Enable for GCA 2.1	Open Drain
GPIO2	GCMA_GPU_WAKE	I	GPU Wake signal for GCA 2.1	10K pull-up to V18_ADM, unless driven actively
GPIO3	HYPER_PSR_PSRN	O	PSR Output to control the PSR power supply	0 to 1V8 Pull-up
GPIO4	GCMA_V18_ADM_EN	O	GPU power sequencing for GCA 2.1	Open Drain
GPIO5	FRM_LCK	I	Active low Frame Lock	1V8 pull-up to FRM_LCK

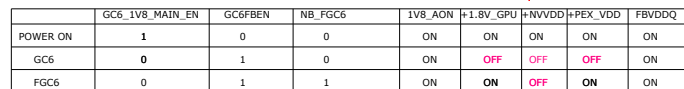
Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

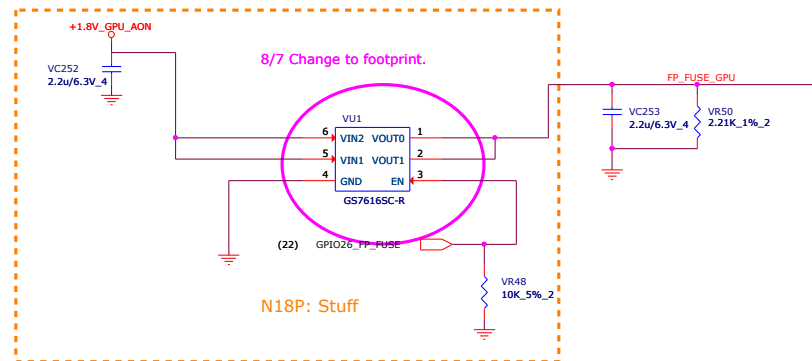
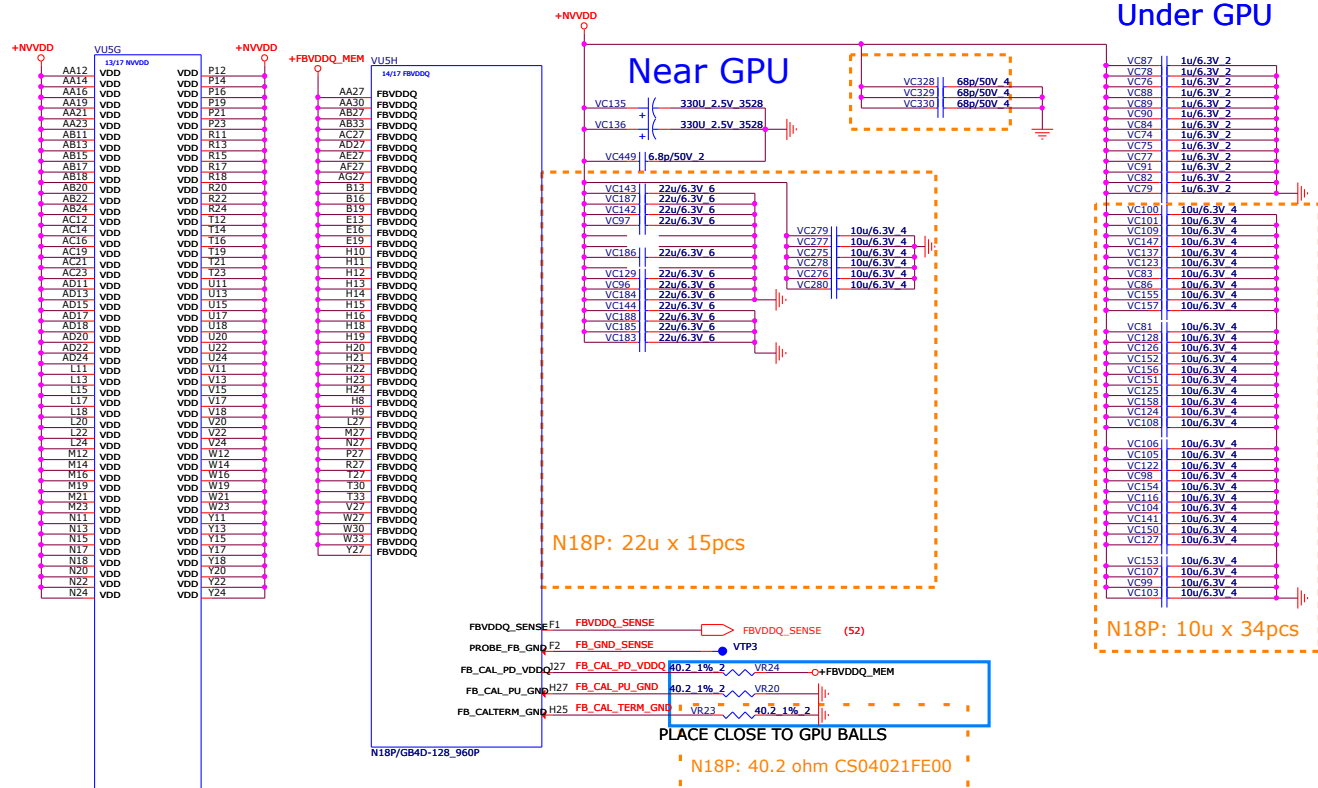
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO6	HYPER_PSR	O	Phase Shifting (see Section 14.3.2)	10K pull-up to V18_ADM to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel backlight enable	10K pull-up to V18_ADM
GPIO8	MEM_VDD_CTL	O	Memory voltage control	10K pull-up to V18_ADM
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain
GPIO10	MEM_VDD_CTL	O	Memory voltage control	10K pull-up to V18_ADM
GPIO11	LCD_VDD	O	Panel Power enable	10K pull-up to V18_ADM
GPIO12	PSR_LEVEL	O	PSR power enable	10K pull-up to V18_ADM
GPIO13	LCD_RELI	O	LCD Panel Reliability Enable	Panel Backlight Enable
GPIO14	HPD_HPD	I	Hot Plug Detect for HPD	Inverted Input. See Figure 14.3
GPIO15	HPD_HPD	I	Hot Plug Detect for HPD	Inverted Input. See Figure 14.3
GPIO16	GCMA_GCA_FR_EN	O	System side PCIe reset monitor	10K pull-up to V18_ADM unless actively driven
GPIO17	HPD_HPD	I	Hot Plug Detect for HPD	Inverted Input. See Figure 14.3
GPIO18	HPD_HPD	O	3D Vision L/R Signal	Inverted Input. See Figure 14.3
GPIO19	3D_VISION	O	3D Vision L/R Signal	10K pull-up to V18_ADM
GPIO20	WAKE_WAKE	I/O	Wake signal	Open Drain
GPIO21	WAKE_WAKE	I/O	Wake signal	Open Drain
GPIO22	WAKE_WAKE	I/O	Wake signal	Open Drain
GPIO23	WAKE_WAKE	I/O	Wake signal	Open Drain

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

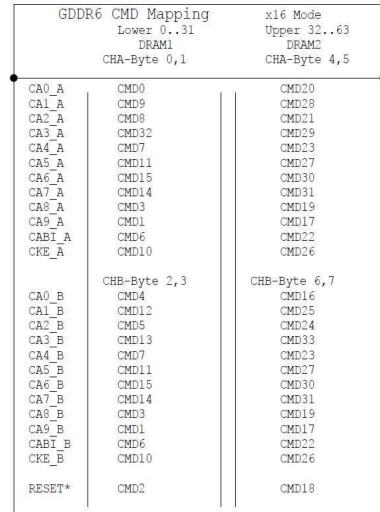
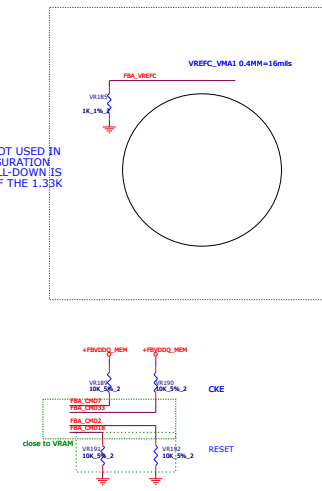
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO24	GCMA_GCA_FR_EN	O	GPU PCIe self-reset control	Open Drain
GPIO25	HPD_HPD	I	Hot plug detect for HPD	Inverted Input. See Figure 14.3
GPIO26	WAKE_WAKE	I/O	Wake signal	Open Drain
GPIO27	WAKE_WAKE	I/O	Wake signal	Open Drain

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	10K pull-up to V18_ADM





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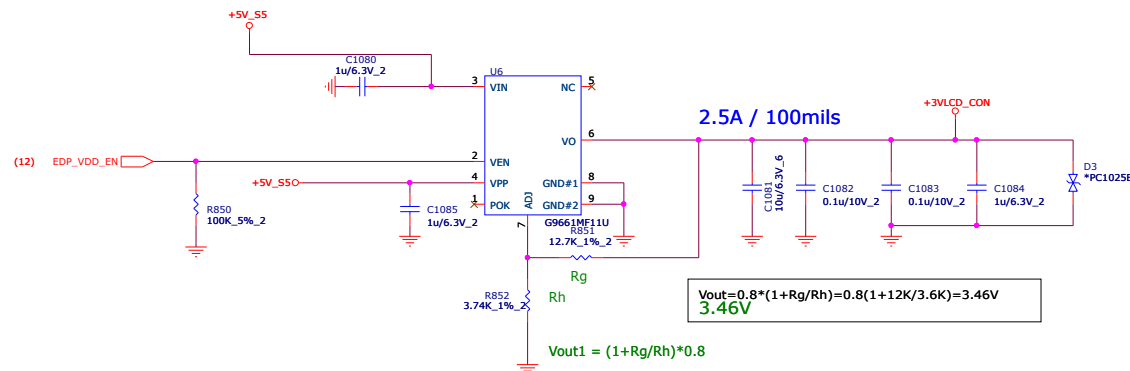
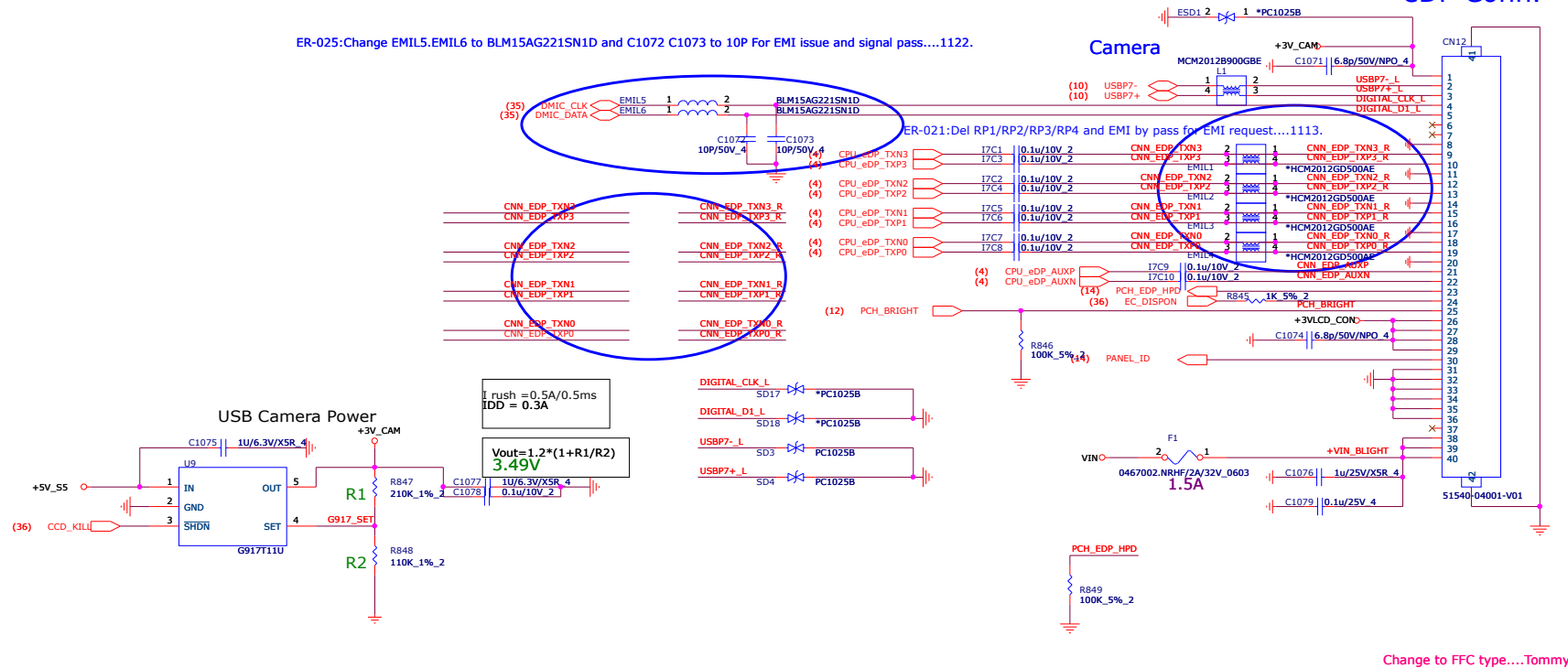


D
C
B
A

D
C
B
A

ER-025:Change EMIL5,EMIL6 to BLM15AG221SN1D and C1072 C1073 to 10P For EMI issue and signal pass....1122.

eDP Conn.



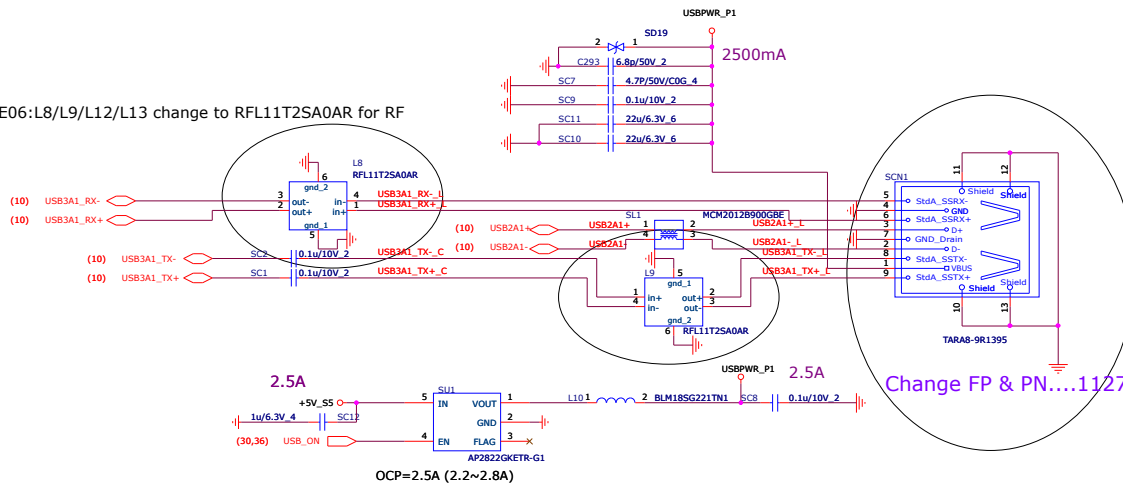
Quanta Computer Inc.
PROJECT : FX506L/FX706L

Size Document Number eDP CONN/CAM/D-MIC Rev 2A
Date: Tuesday, March 24, 2020 Sheet 28 of 59

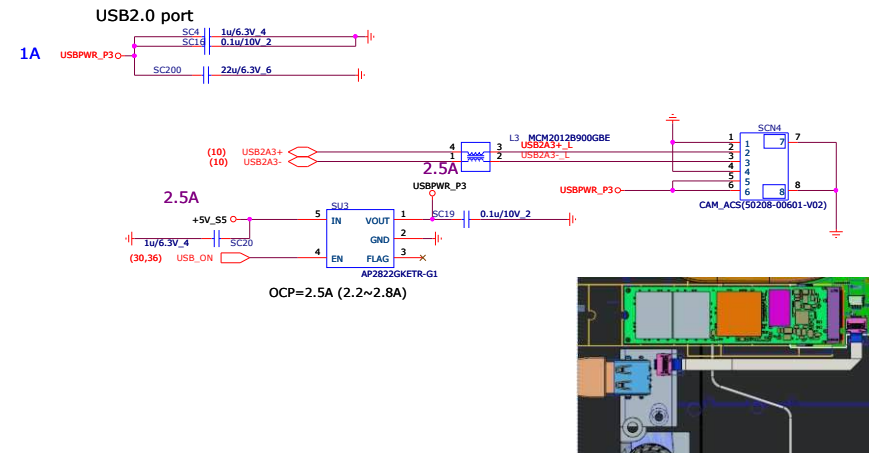
USB 3.2 GEN1 Type A/ PORT1

USB 2.0 PORT1

PR-E06:L8/L9/L12/L13 change to RFL11T2SA0AR for RF

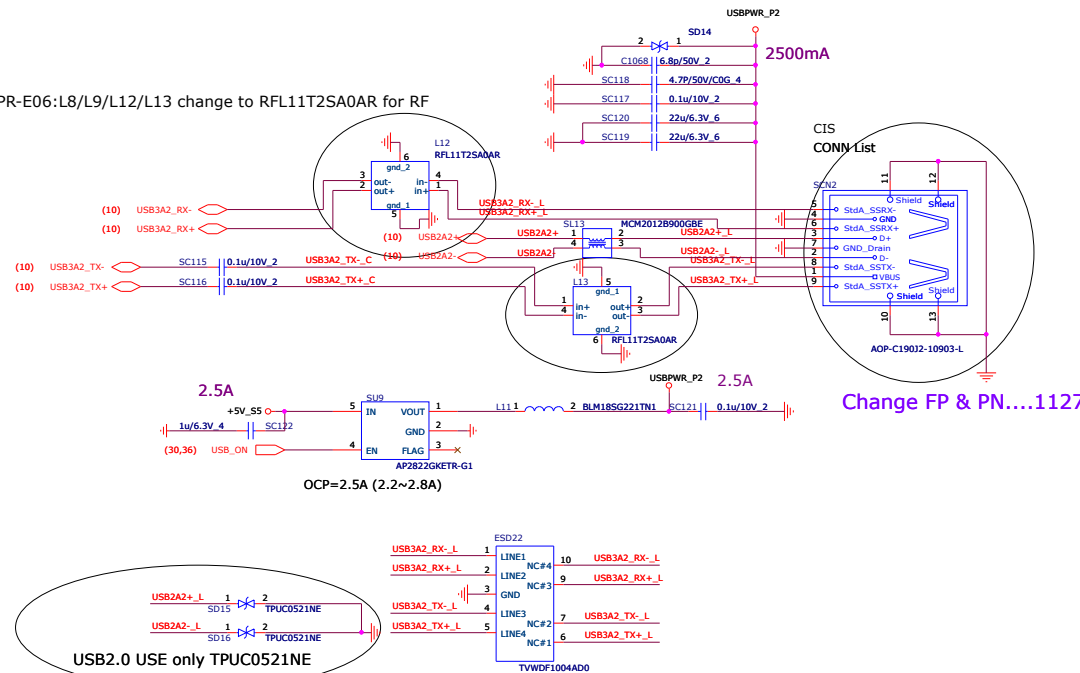


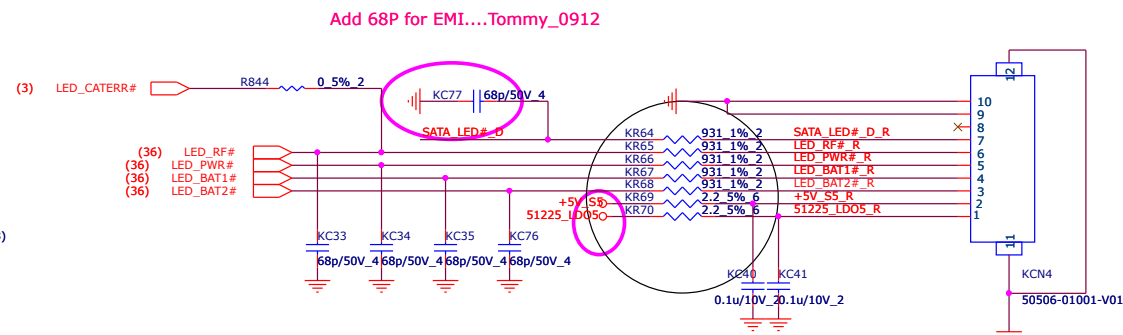
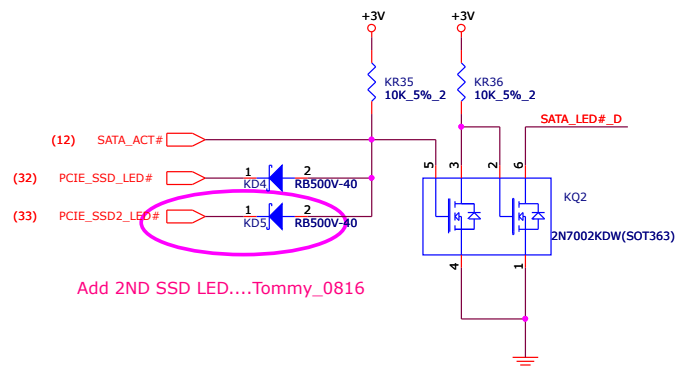
PR-E02:Remove CON6 for USB board FFC CONN.....0217



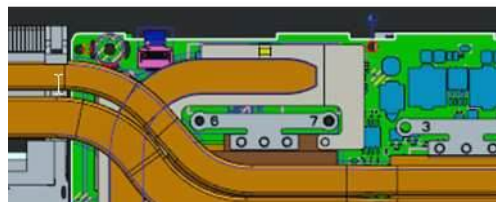
USB 3.2 GEN1 Type A/PORT2

PR-E06:L8/L9/L12/L13 change to RFL11T2SA0AR for RF





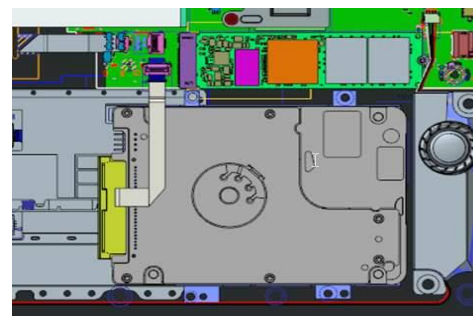
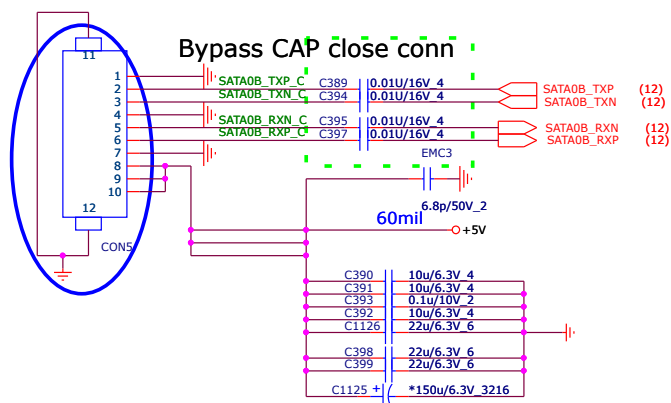
ER-E34:KR64, KR65, KR66, KR67, KR68 change from 390 to 931 ohm for brightness



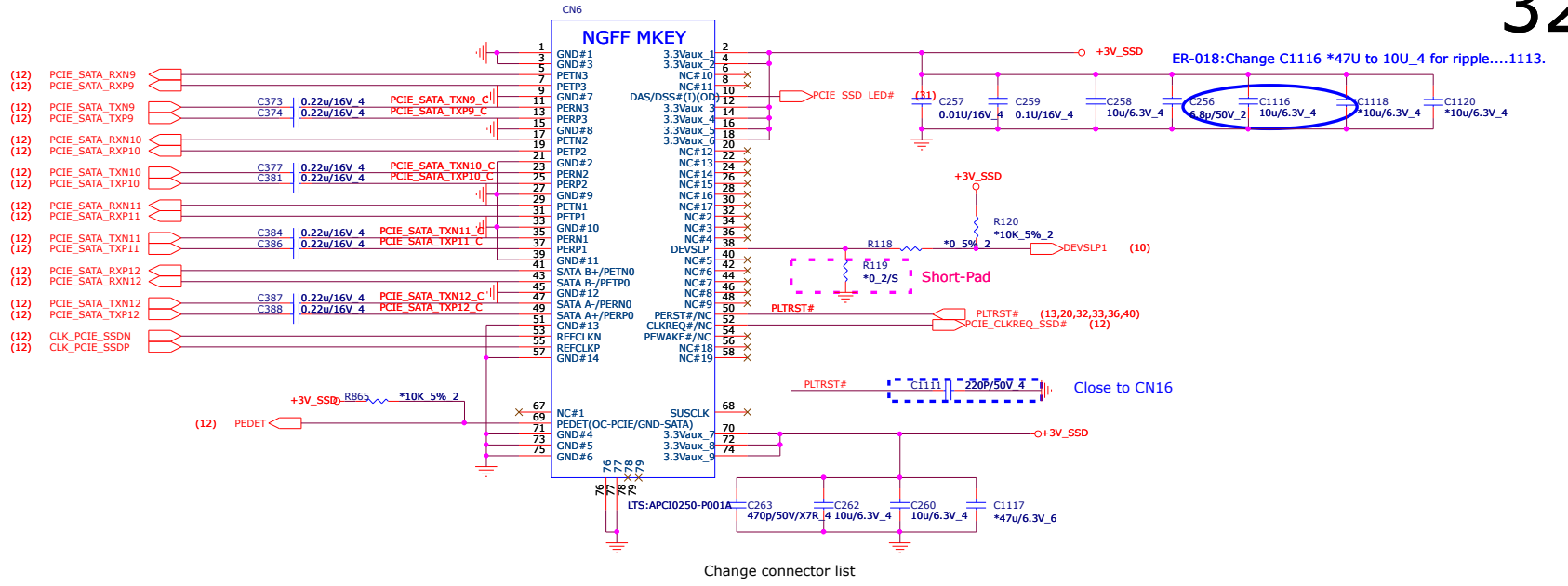
SATA HDD FFC

ER-032:Change HDD FFC pin define for ME cable routing....1126

ACS:51647-01001-V02

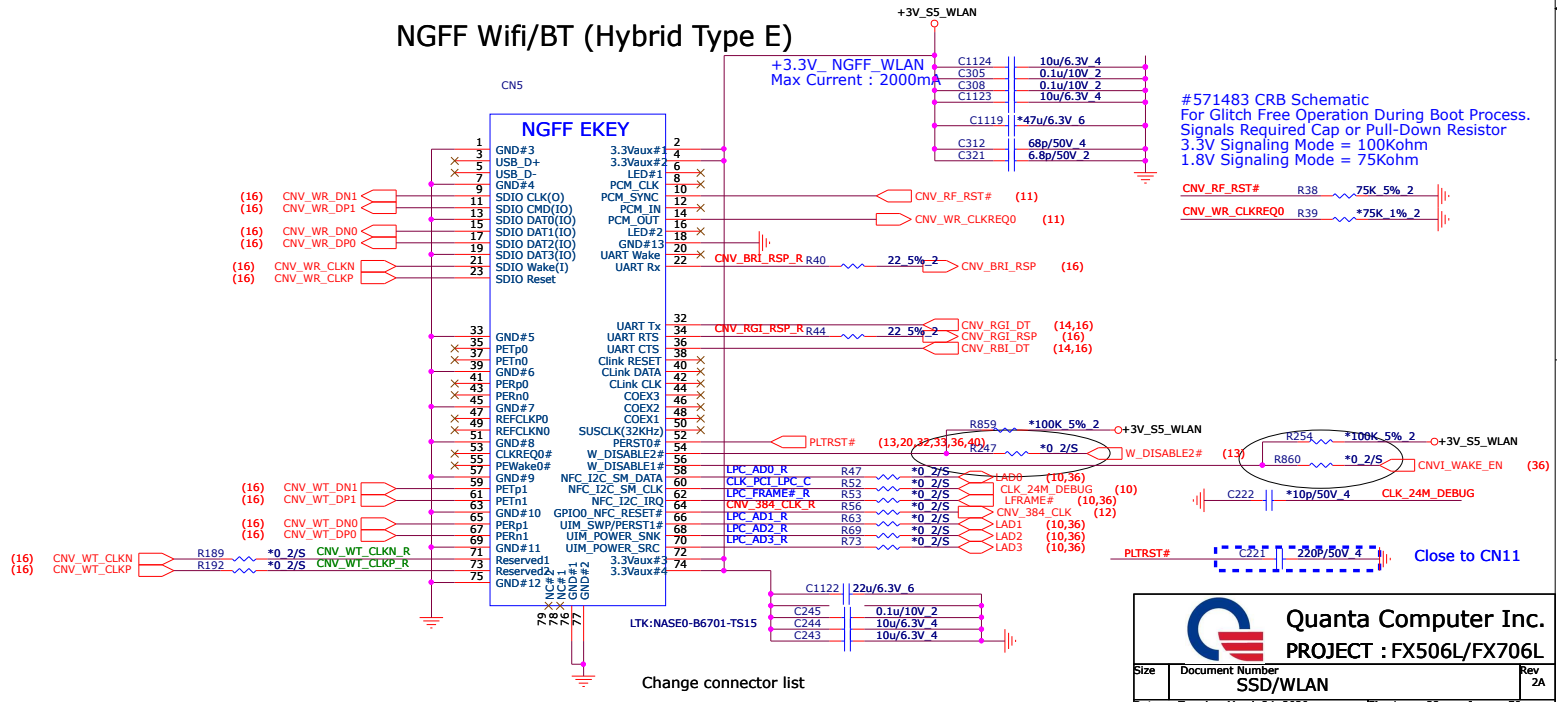


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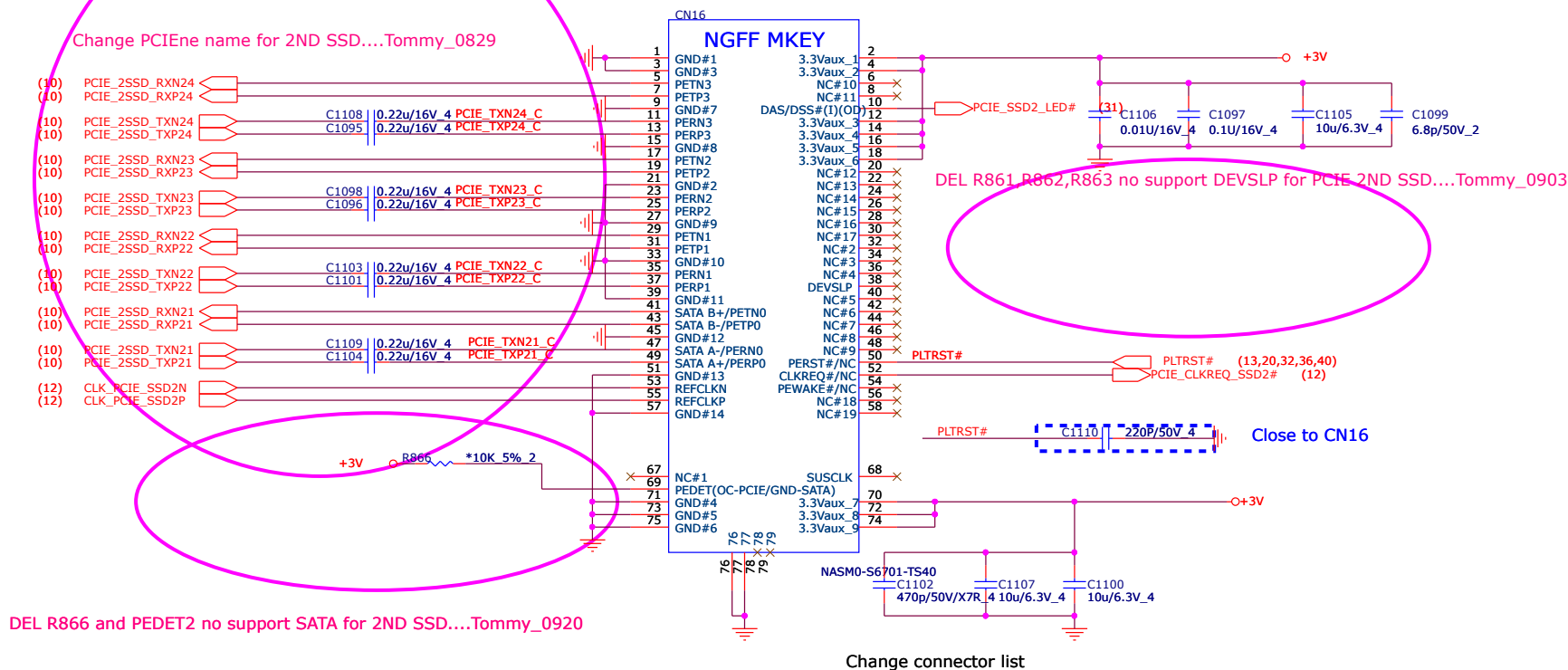


WLAN/BT

NGFF Wifi/BT (Hybrid Type E)

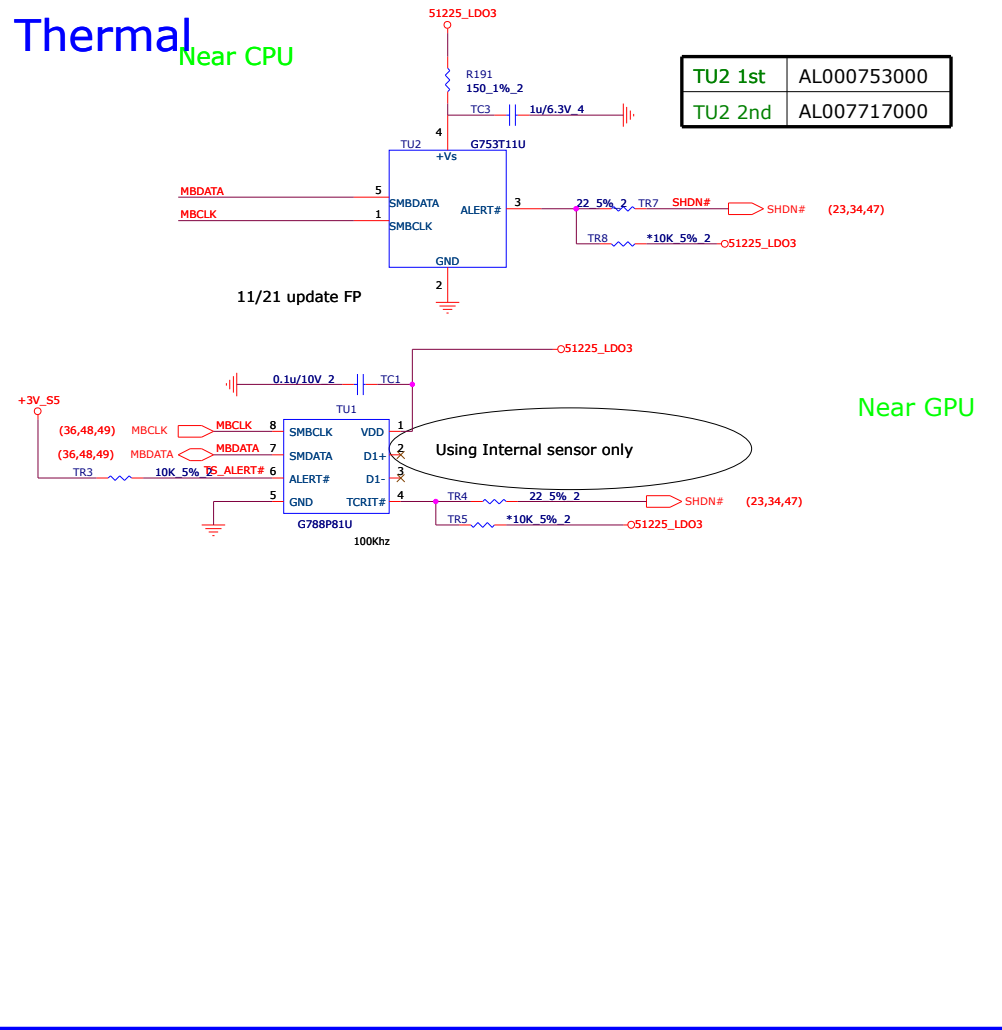


2ND SSD



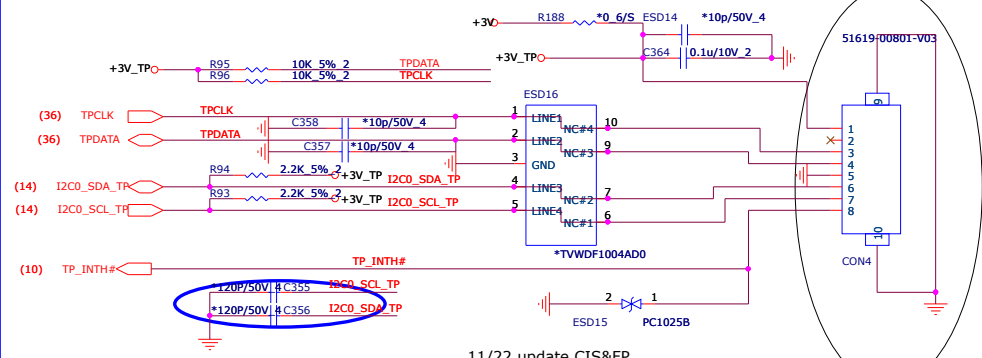
Thermal

Near CPU



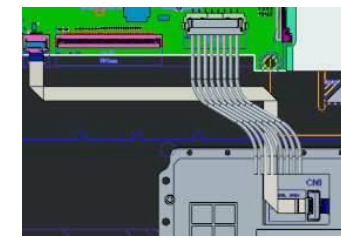
Near GPU

Touch Pad Connector AA type

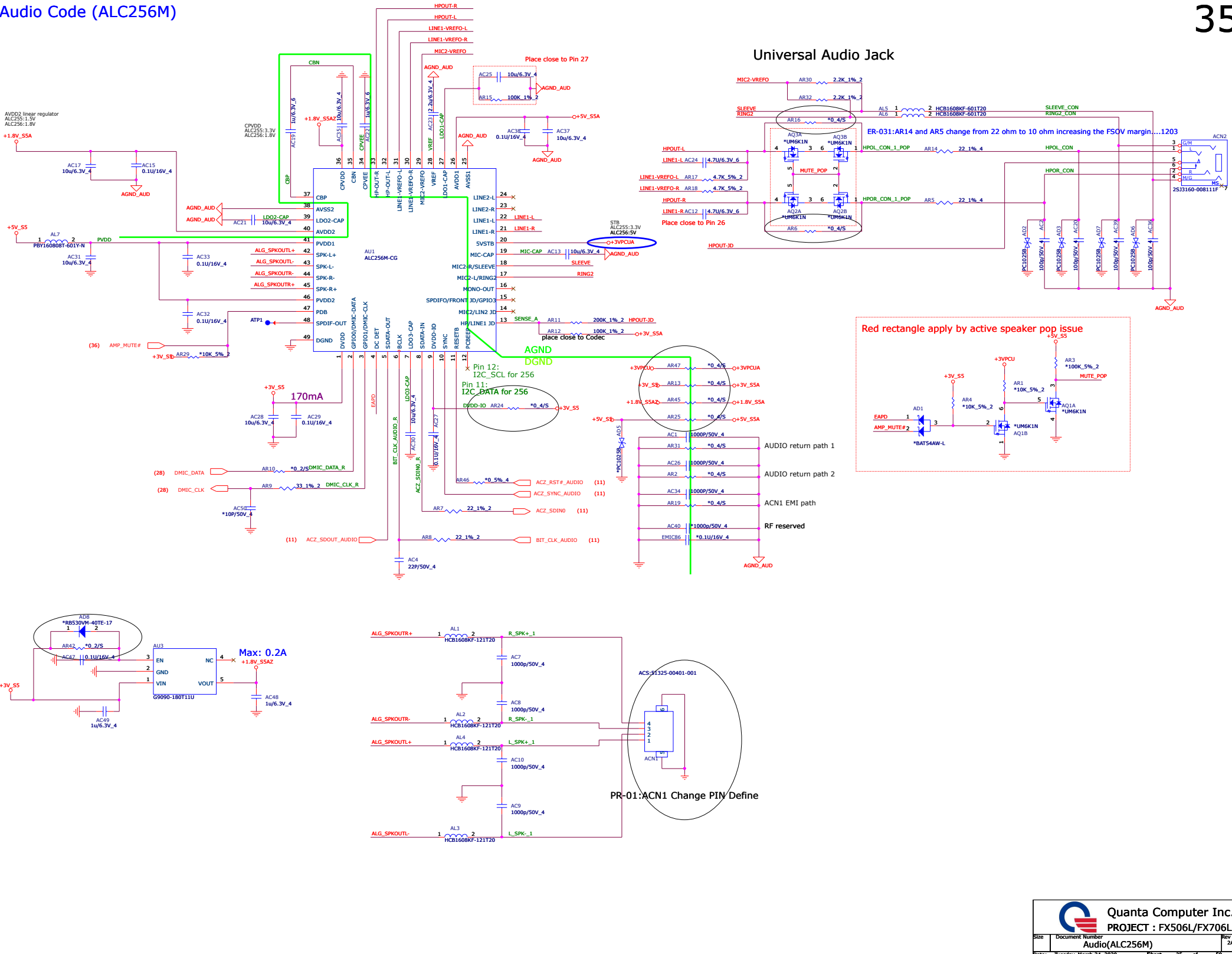


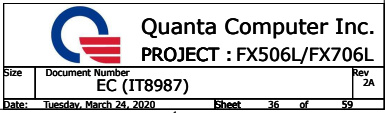
ER-029: Change C355,C356 to no-mount for fix TP timing issue....1122.

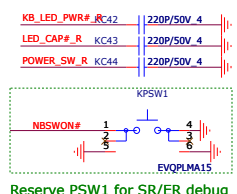
Change connector list



Audio Code (ALC256M)

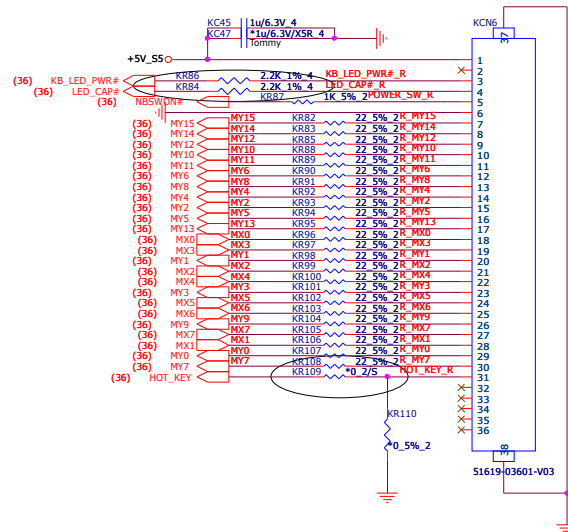
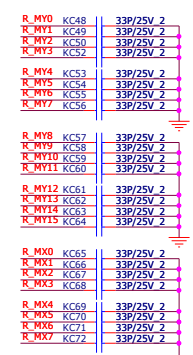






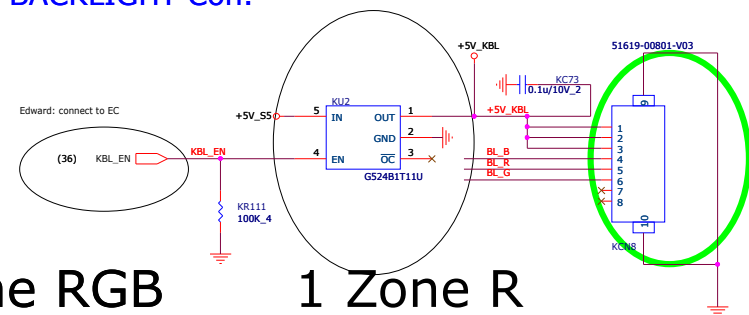
KEYBOARD Con.

PR-E10:KR84, KR86 change from 220 ohm to 2.2K ohm for ID KB LED brightness request.



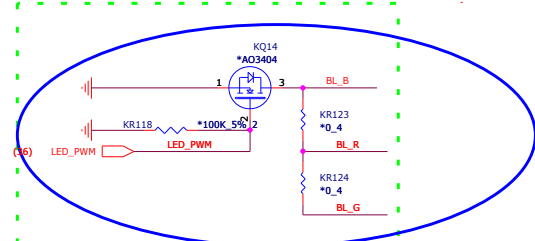
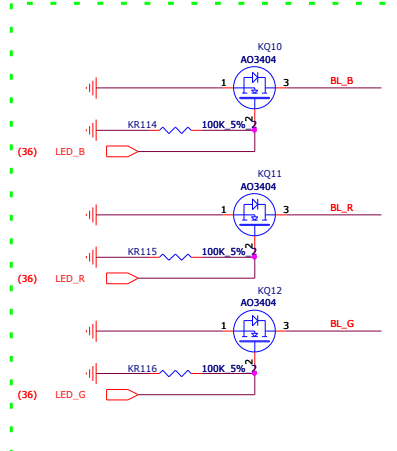
KEYBOARD BACKLIGHT Con.

8/7 Change to footprint.



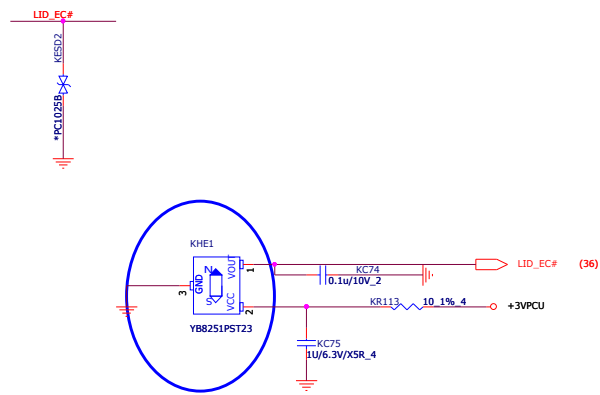
1 Zone RGB

1 Zone R



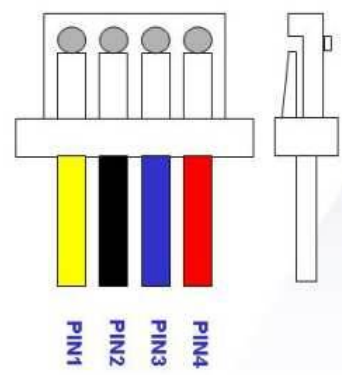
ER-031:Del KQ15/KQ13 for no support Red backlight....1125.

ESD23 CLOSE TO KHE1



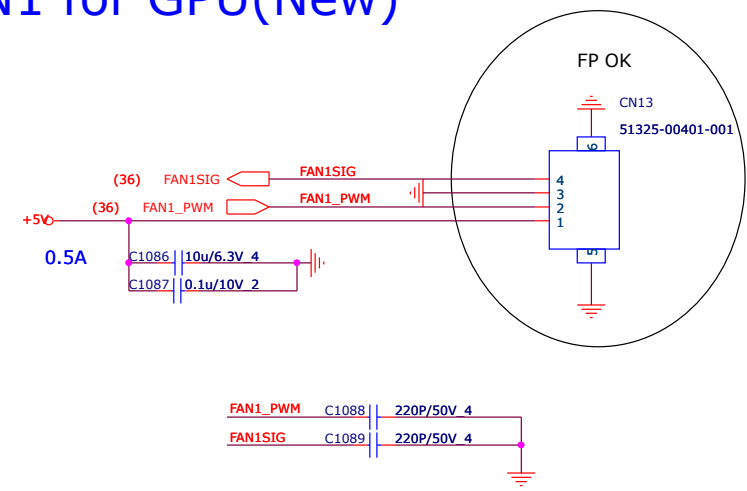
ER-033:Change footprint for SMT request....1126.

4Pins Fan Connector Pins Definition

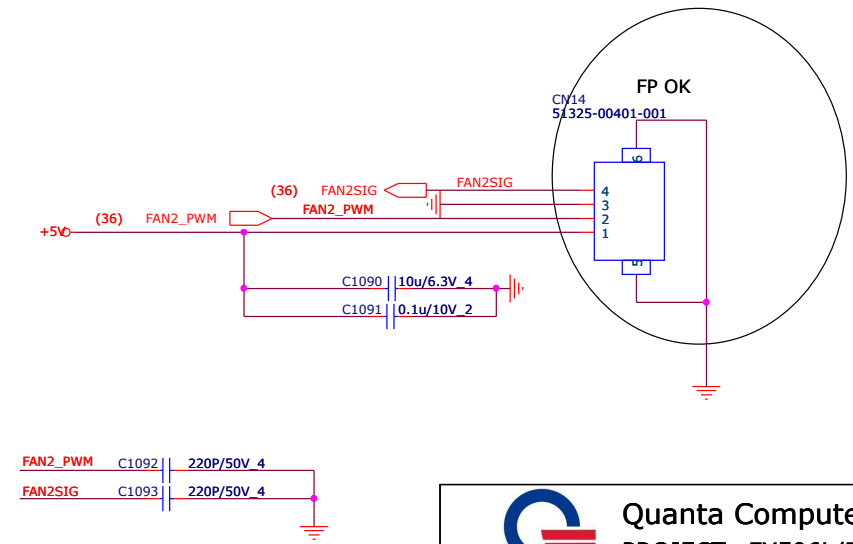


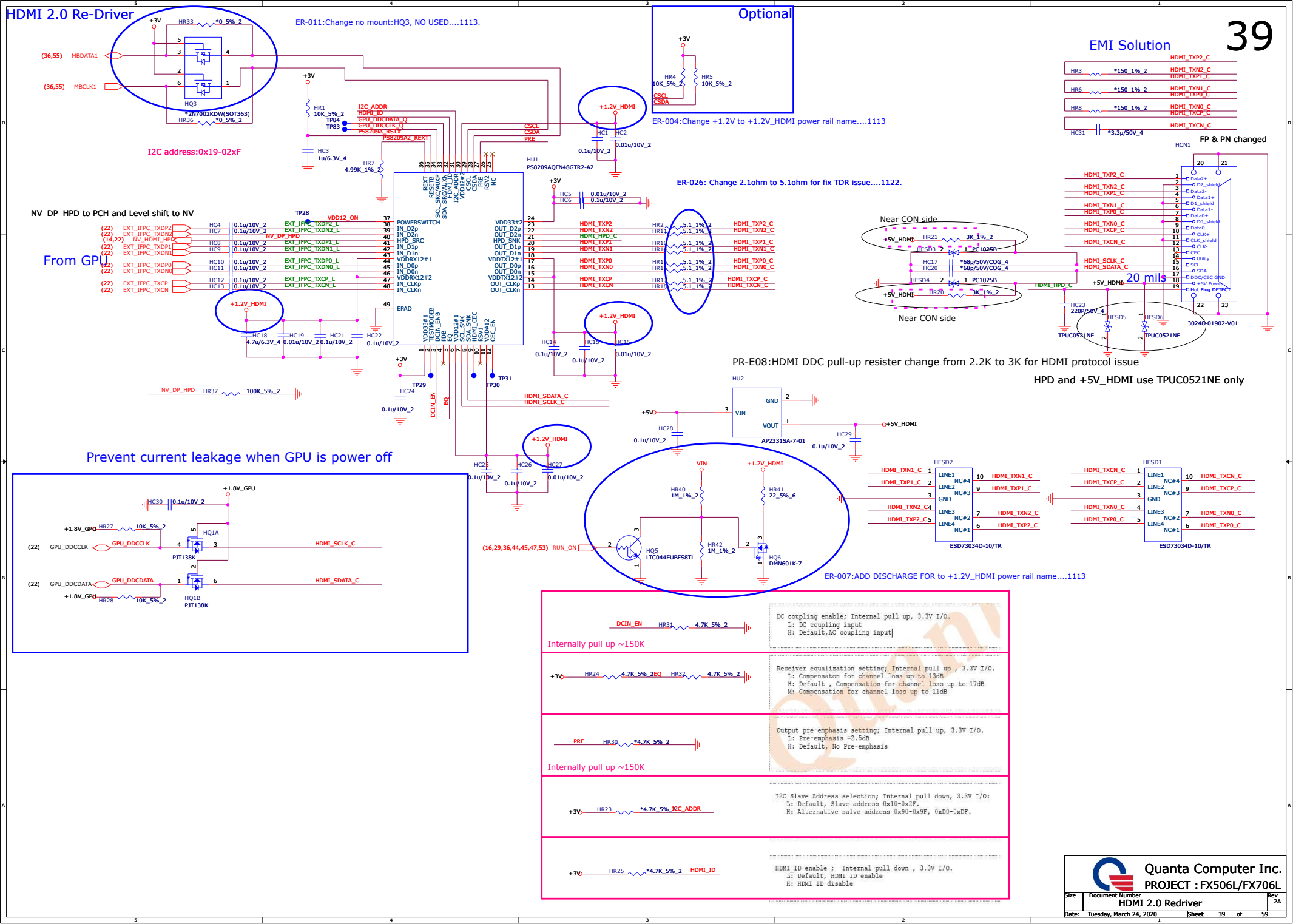
Pin No.	Function
Pin 1	TACHO
Pin 2	GNA
Pin 3	PWM
Pin 4	+5V

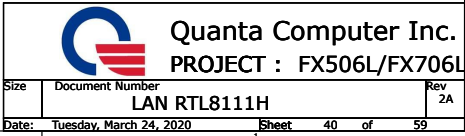
FAN1 for GPU(New)



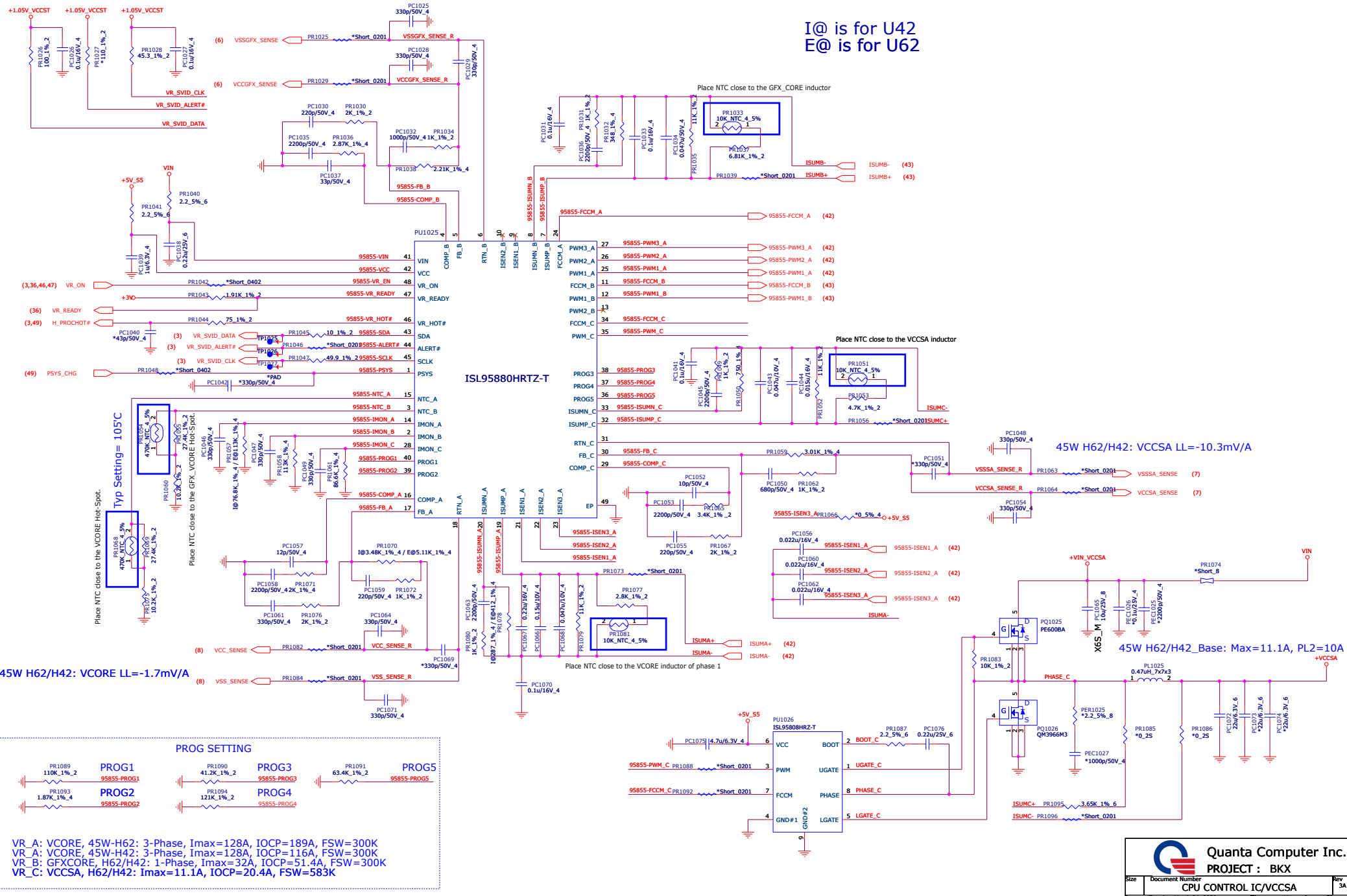
FAN2 for CPU







45W H62/H42: GFX_CORE LL=-2.7mV/A

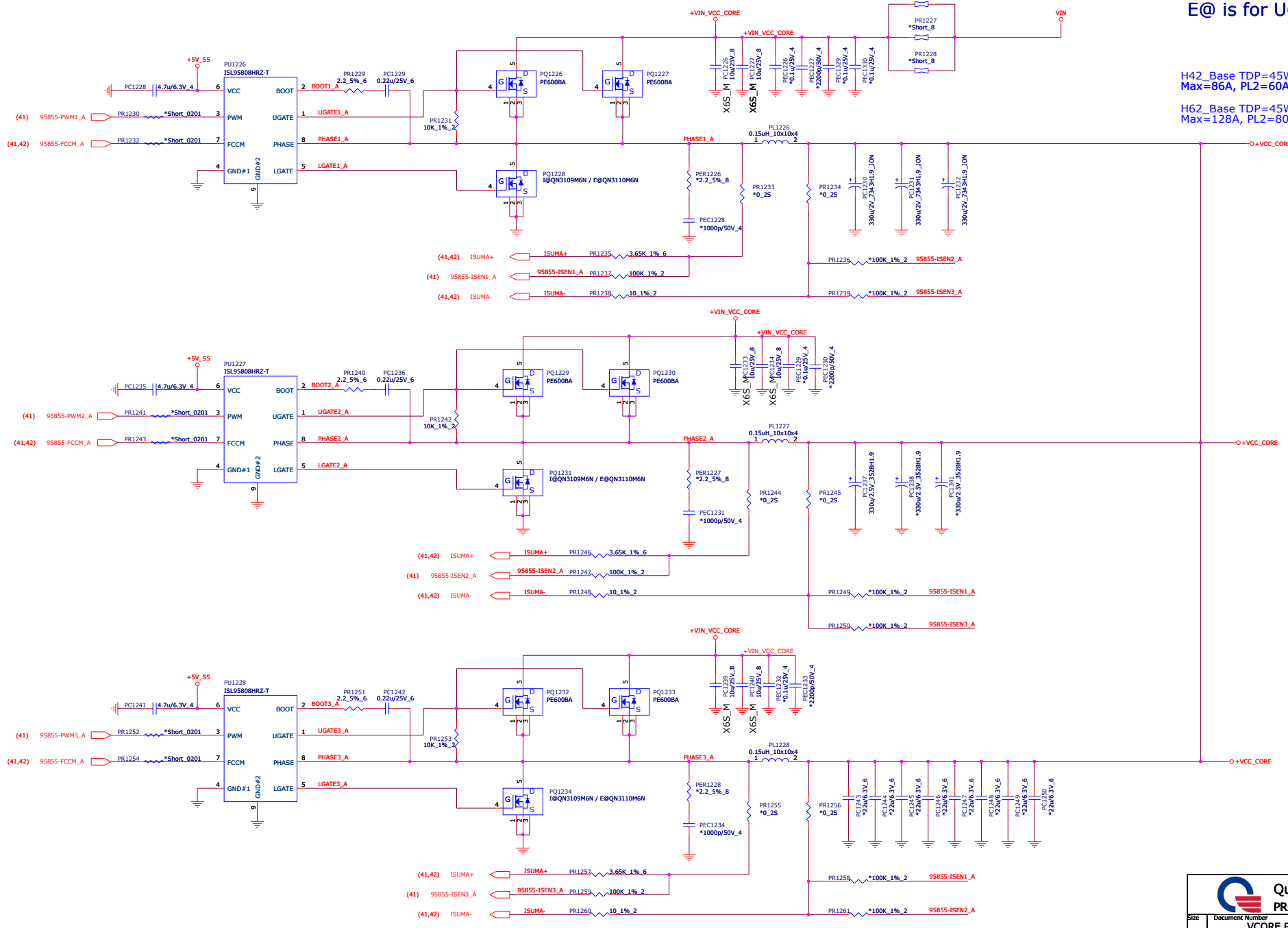


VCORE

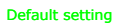
I@ is for U42
E@ is for U62

H42_Base TDP=45W:
Max=86A, PL2=60A, LL=1.7m

H62_Base TDP=45W:
Max=128A, PL2=80A, LL=1.7m



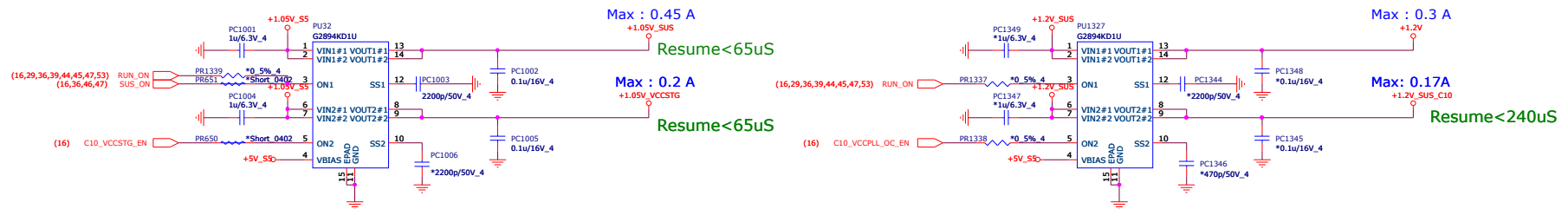
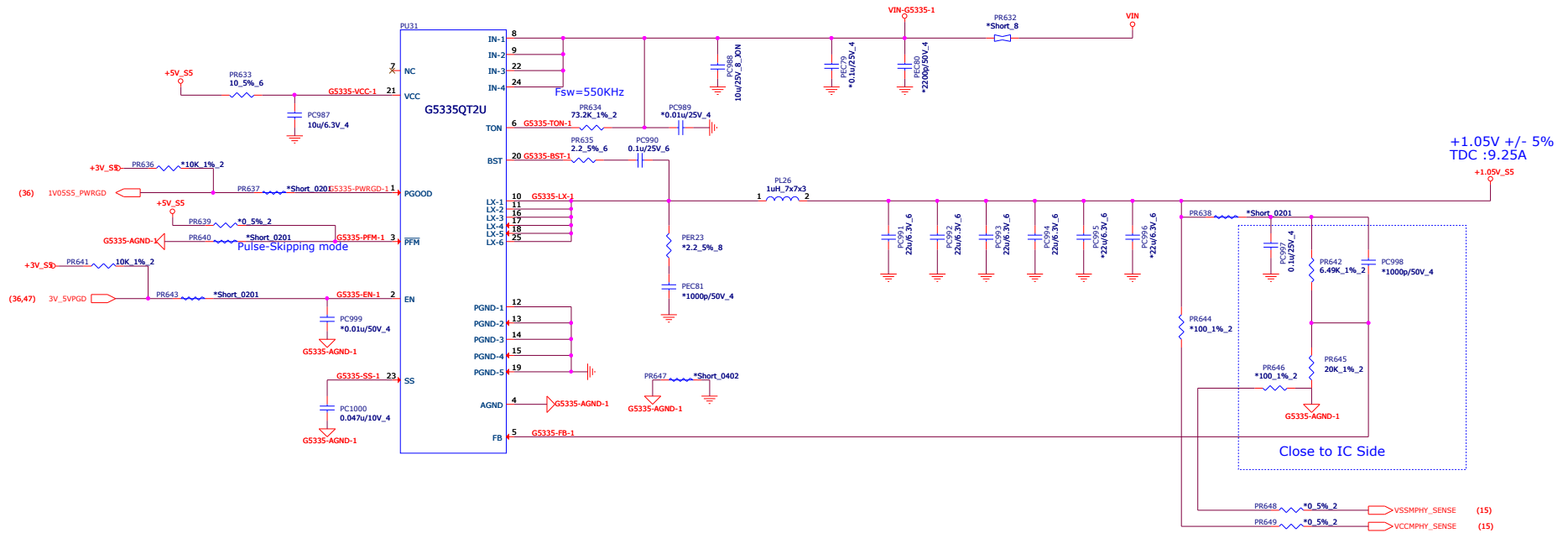
Default setting



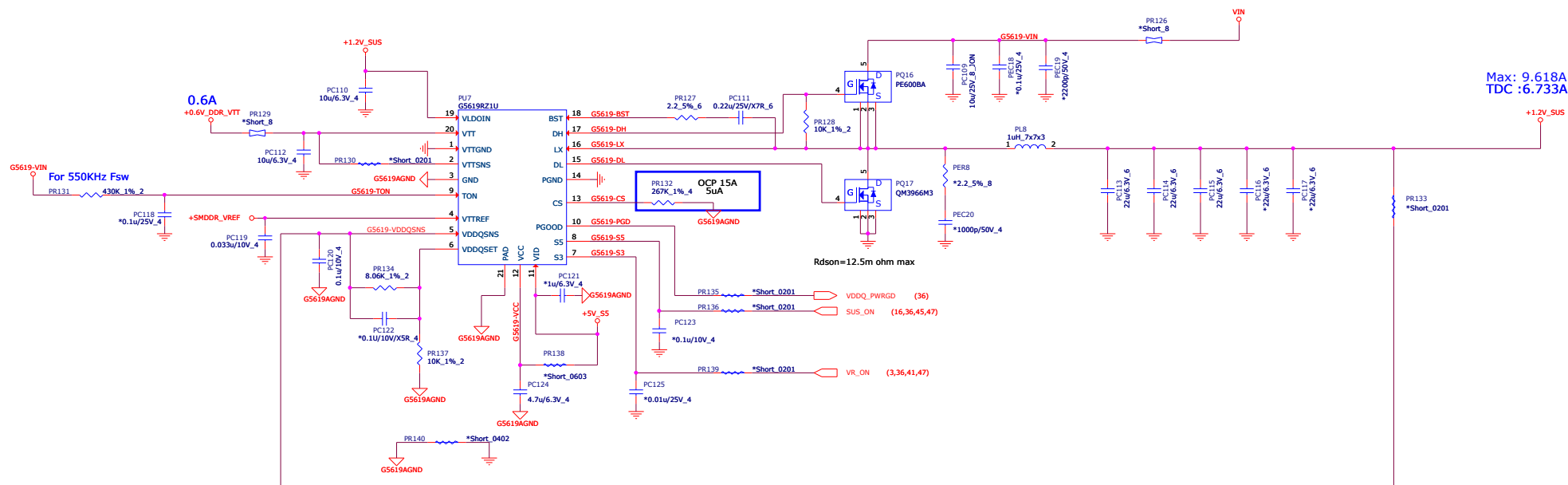
VID0_VCCIO	VID1_VCCIO	LP#	VCCIO
X	X	0	0V
0	0	1	0.85V
1	0	1	0.875V
0	1 (IC internal PU High)	1	0.95V

Default setting

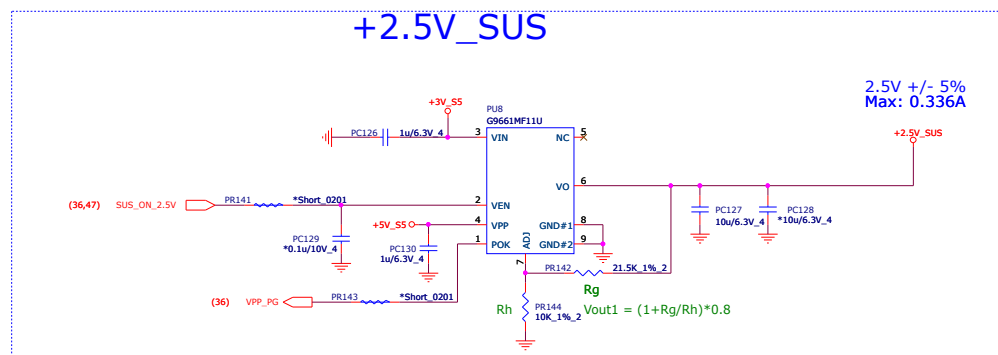
+1.05V_S5



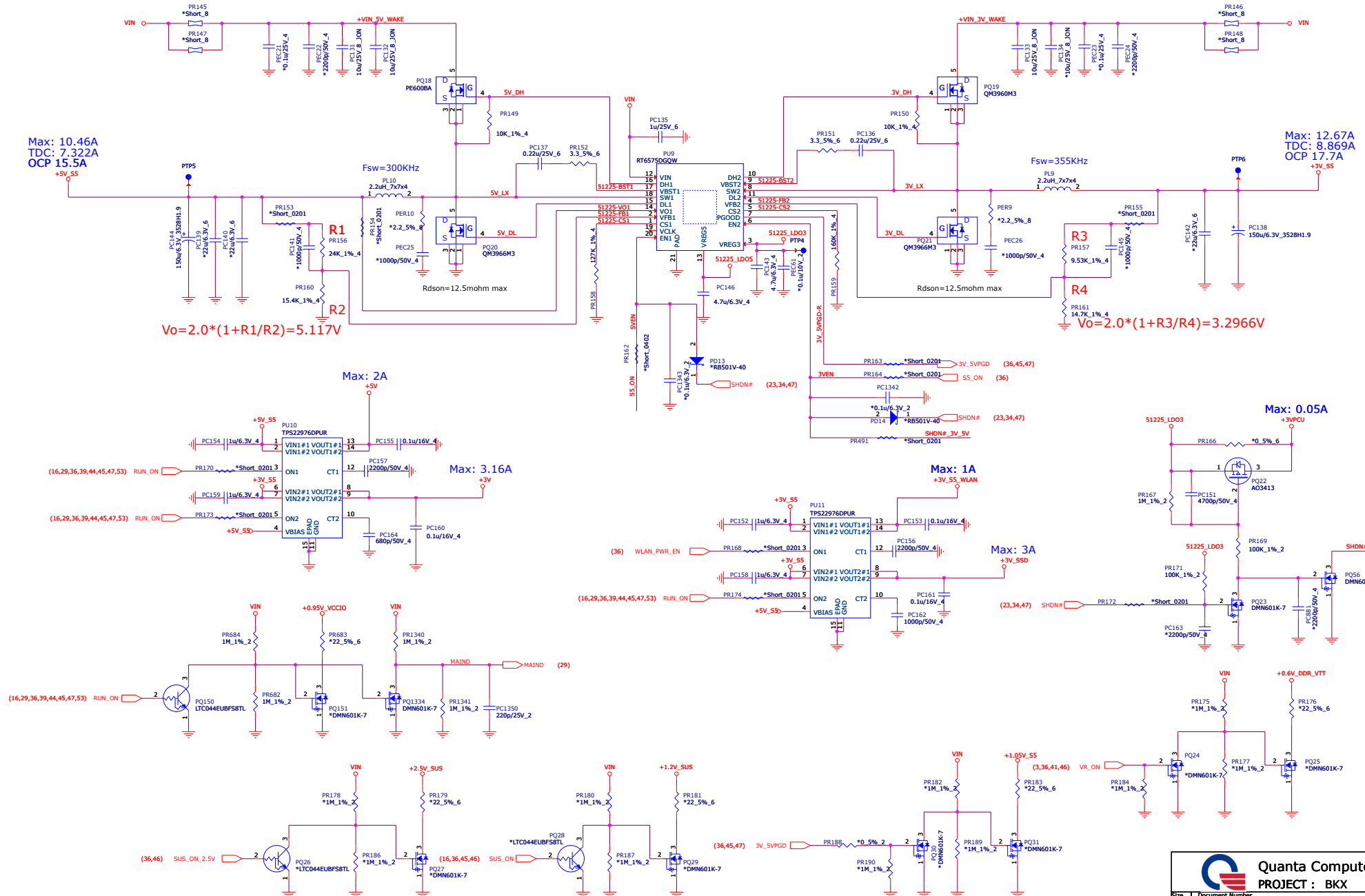
1.2VSUS & VTT_MEM



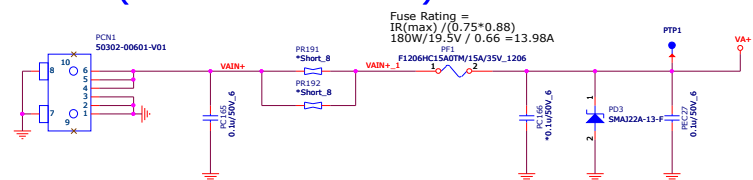
STATE	S3	S5	+1.2V_SUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off



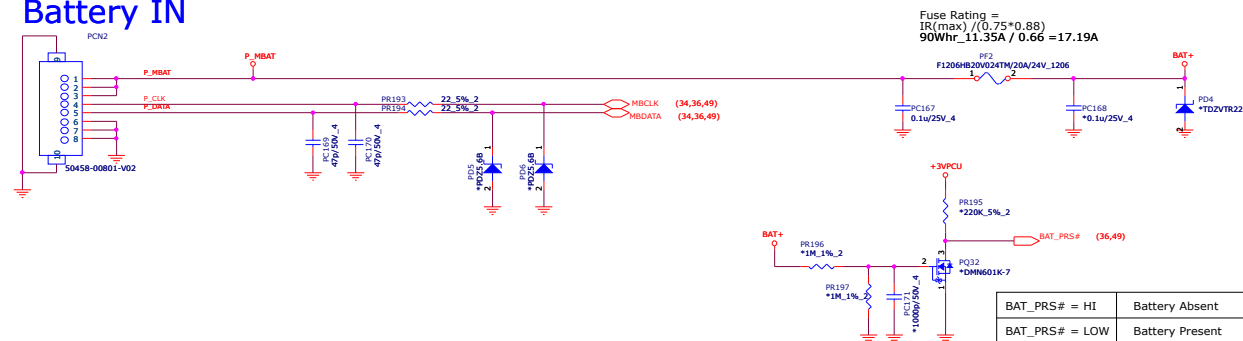
3.3V & 5V

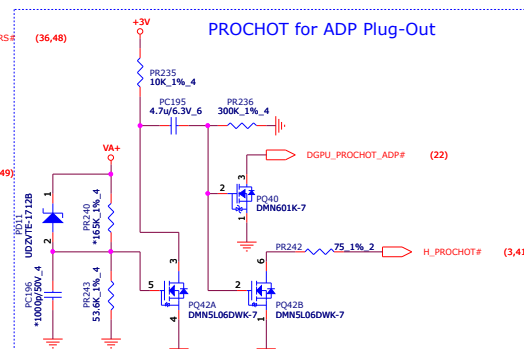


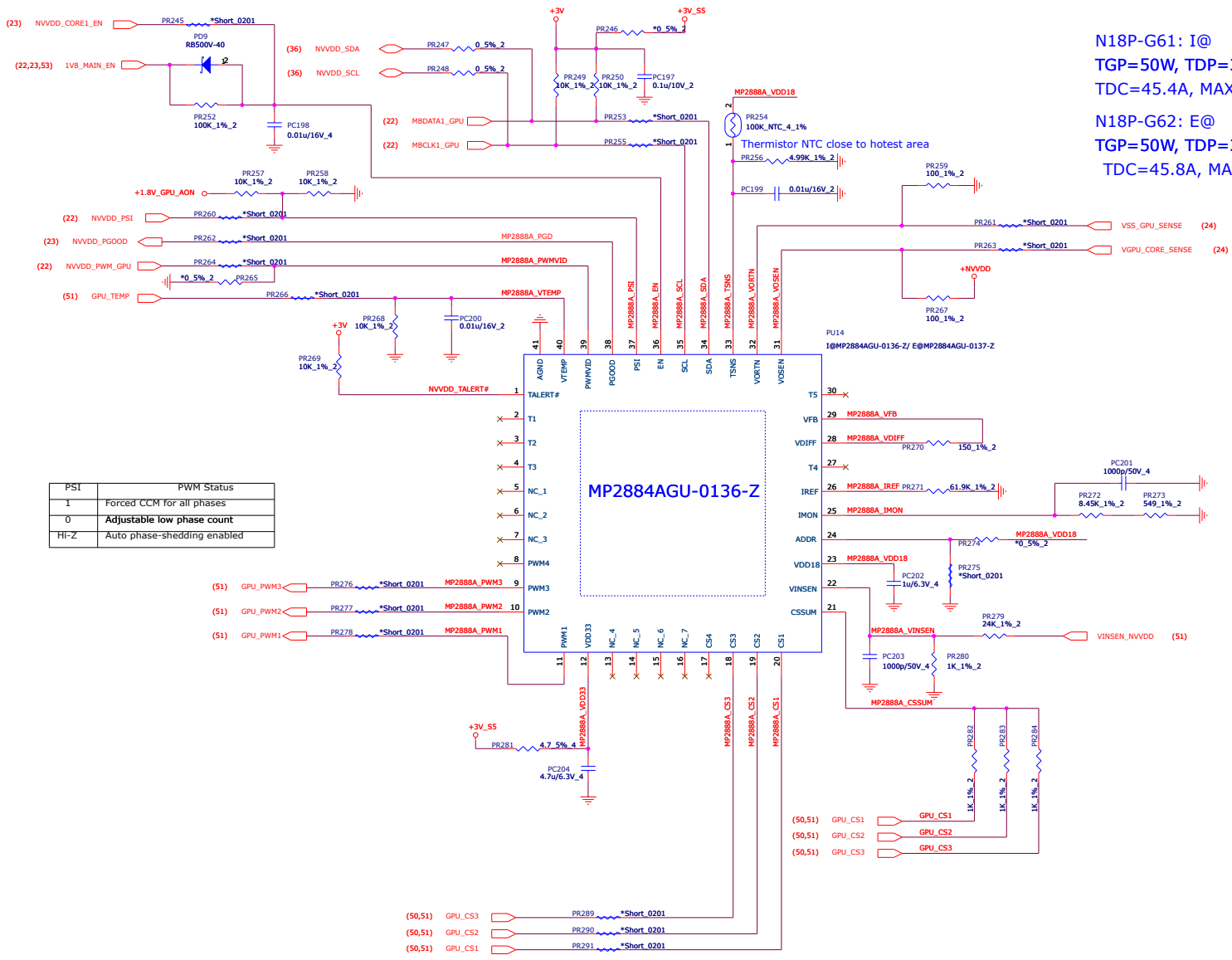
AC IN (On-Board DC-Jack)



Battery IN

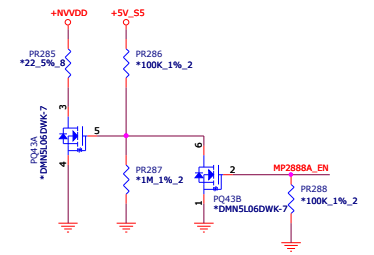






N18P-G61: I@
TGP=50W, TDP=36W
TDC=45.4A, MAX=100.2A
N18P-G62: E@
TGP=50W, TDP=36.1W
TDC=45.8A, MAX=120.5A

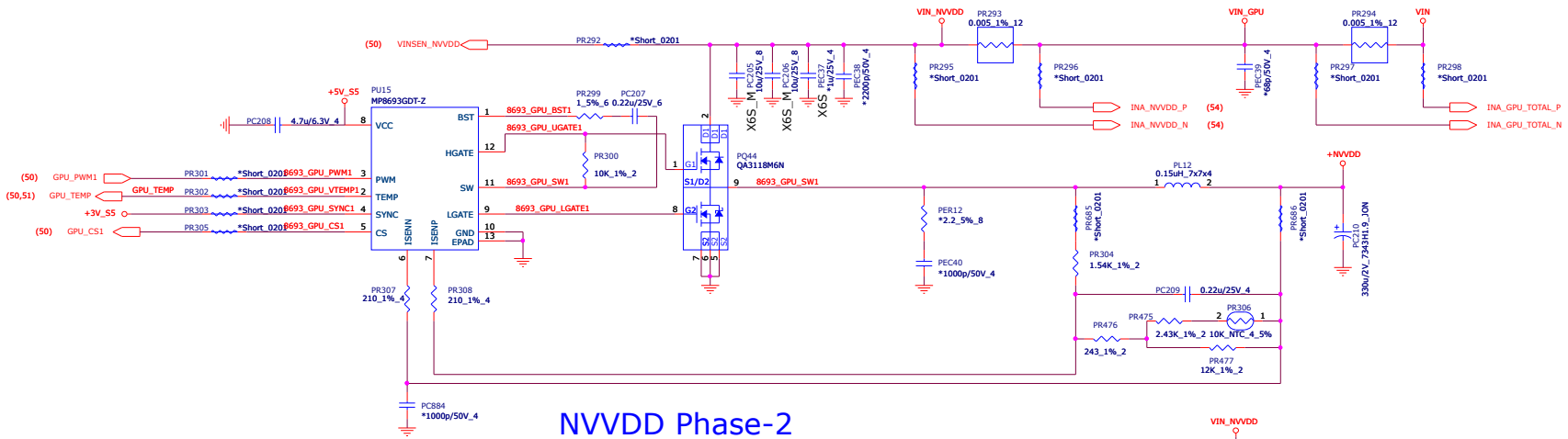
PS1	PWM Status
1	Forced CCM for all phases
0	Adjustable low phase count
Hi-Z	Auto phase-shedding enabled



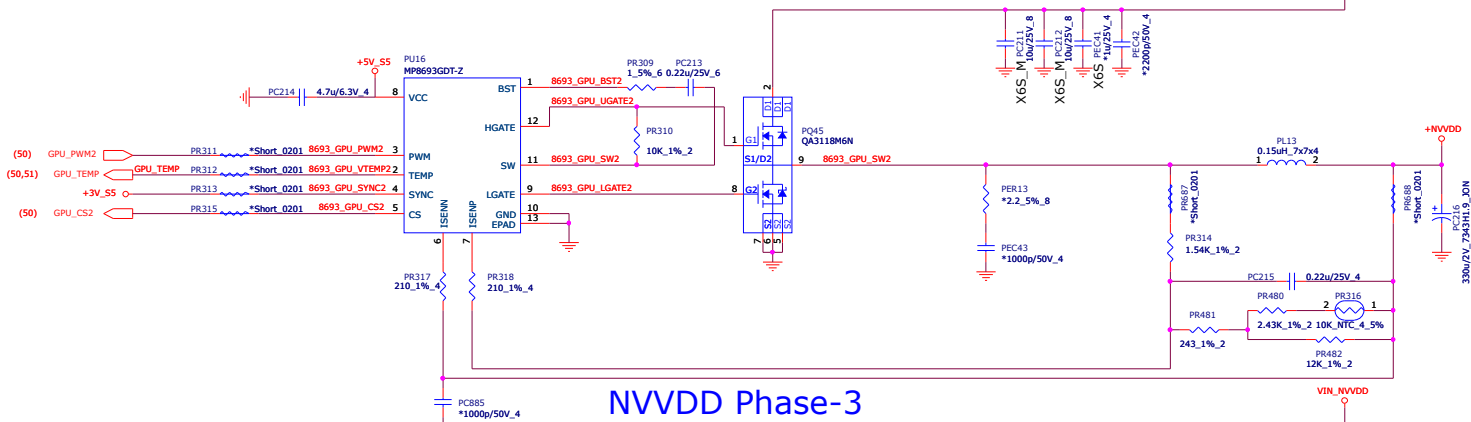
NVVDD Phase-1

N18P-G61
TGP=50W, TDP=36W
TDC=45.4A, MAX=100.2A

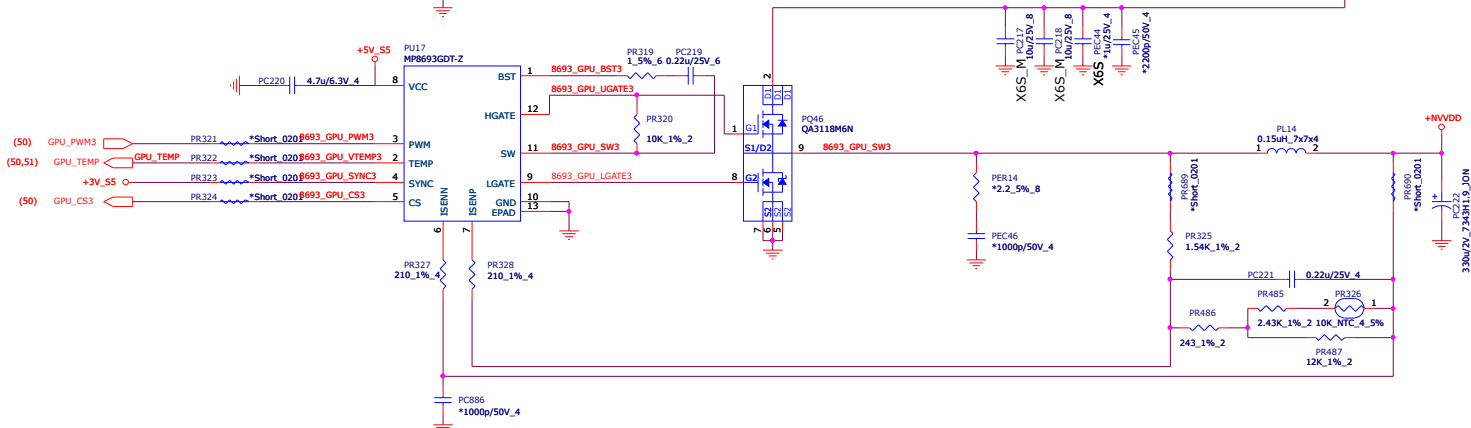
N18P-G62
TGP=50W, TDP=36.1W
TDC=45.8A, MAX=120.5A



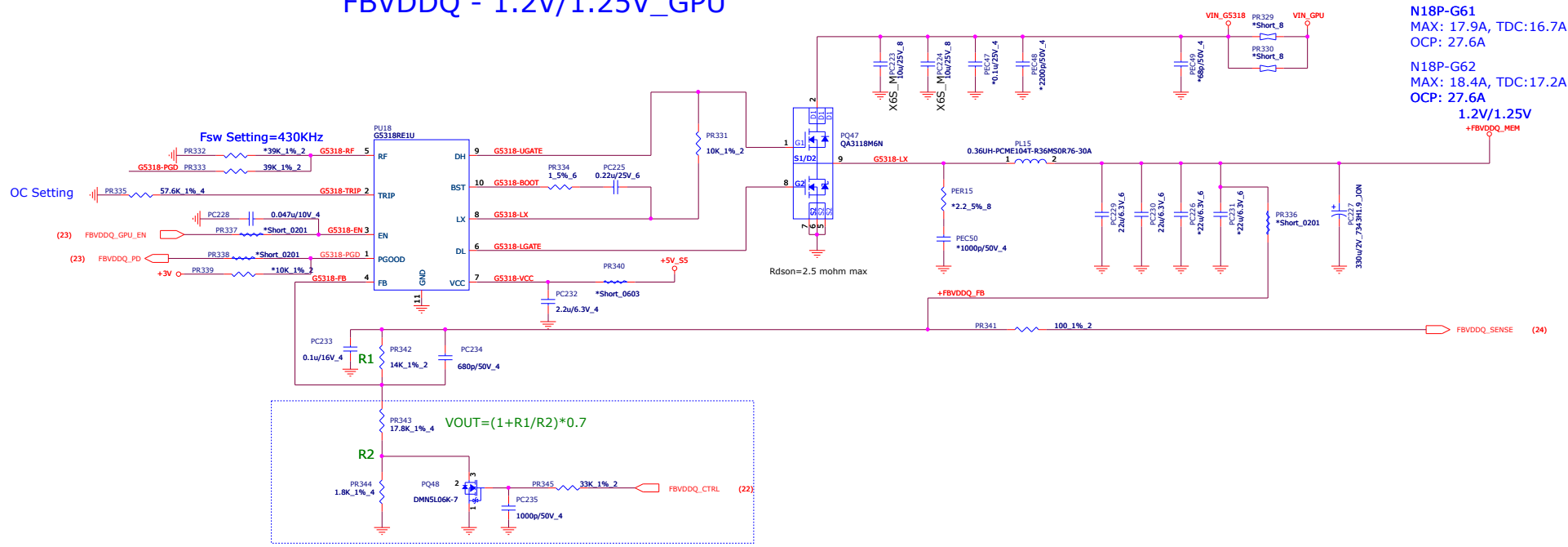
NVVDD Phase-2



NVVDD Phase-3



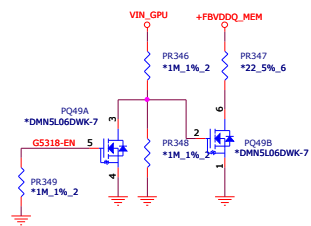
FBVDDQ - 1.2V/1.25V_GPU



N18P-G61
MAX: 17.9A, TDC:16.7A
OCP: 27.6A
N18P-G62
MAX: 18.4A, TDC:17.2A
OCP: 27.6A
1.2V/1.25V
+FBVDDQ_MEM

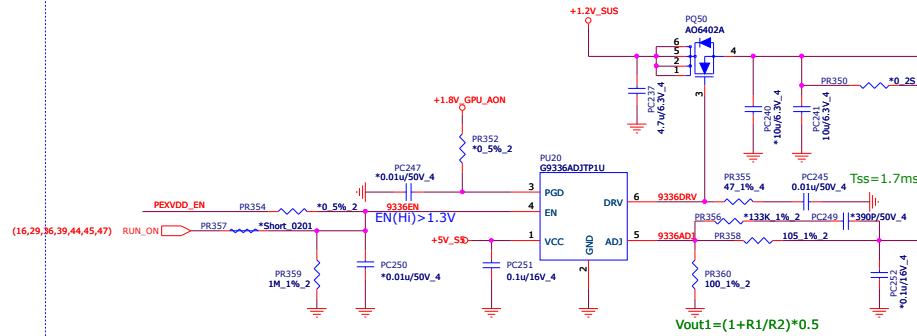
FBVDDQ Voltage Setting: 1.20V / 1.25V for MICRON & SAMSUNG VRAM

FBVDDQ_CTRL	PR343	PR344	FBVDDQ
1	17.8K(CS31782FB10)	1.8K(CS21802FB10)	1.25V
0	17.8K(CS31782FB10)	1.8K(CS21802FB10)	1.2V



+1.0V_GPU

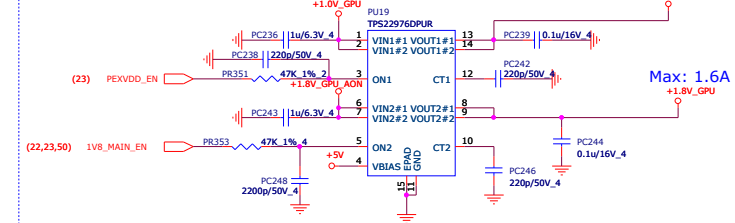
1.0V
TDC: 1.6A
Max: 1.9A



Load Switch for GPU

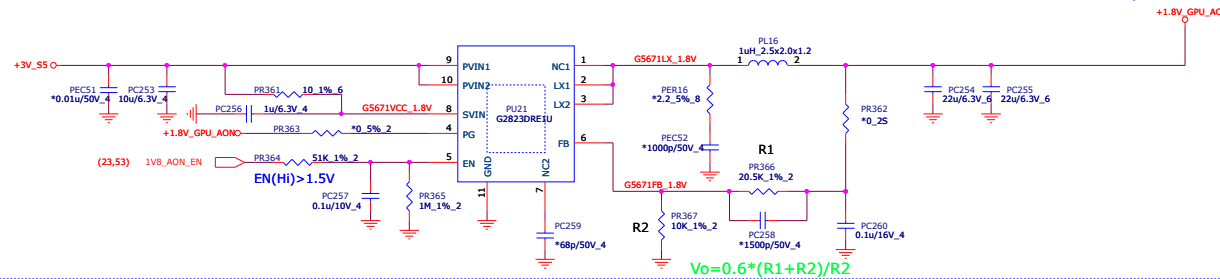
Max: 1.9A
+PEX_VDD

Max: 1.6A
+1.8V_GPU



+1.8V_GPU_AON

1.8V +/- 5%
OCP: Min 4A
TDC: 1.7A
Max: 2A



1V8_GPU_AON

1V8_MAIN_EN

+1.8V_GPU

NVVD

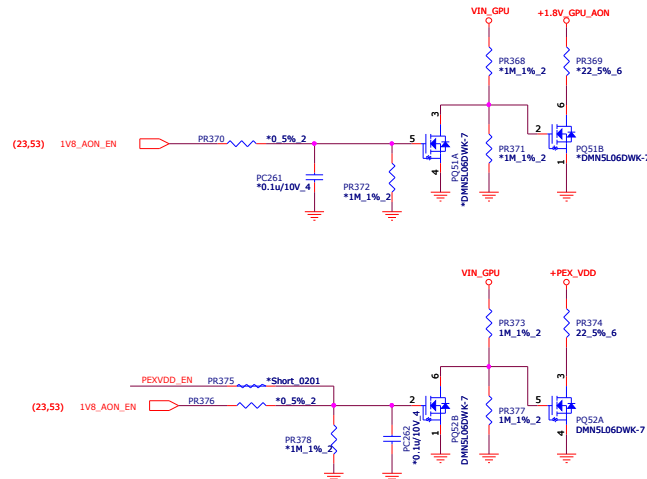
PEX_VDD

FBVDDQ

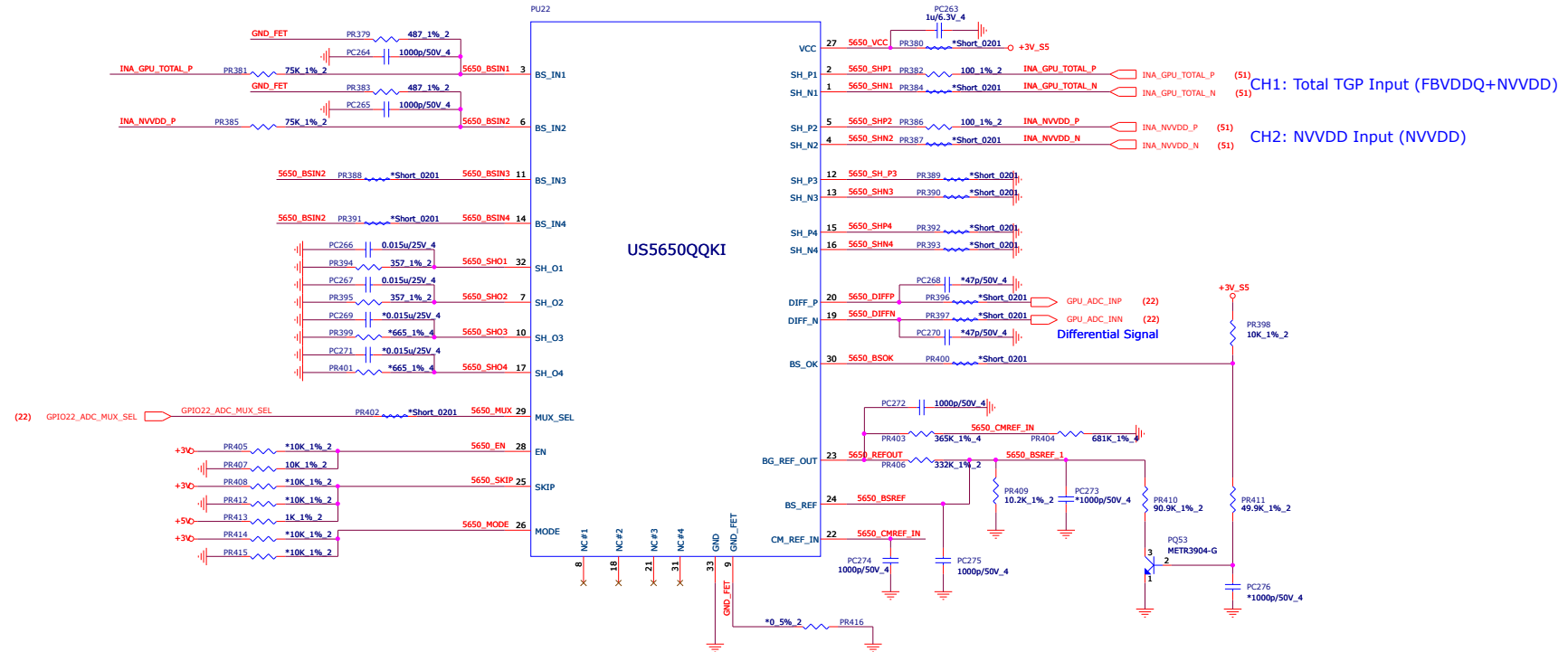
< 4ms

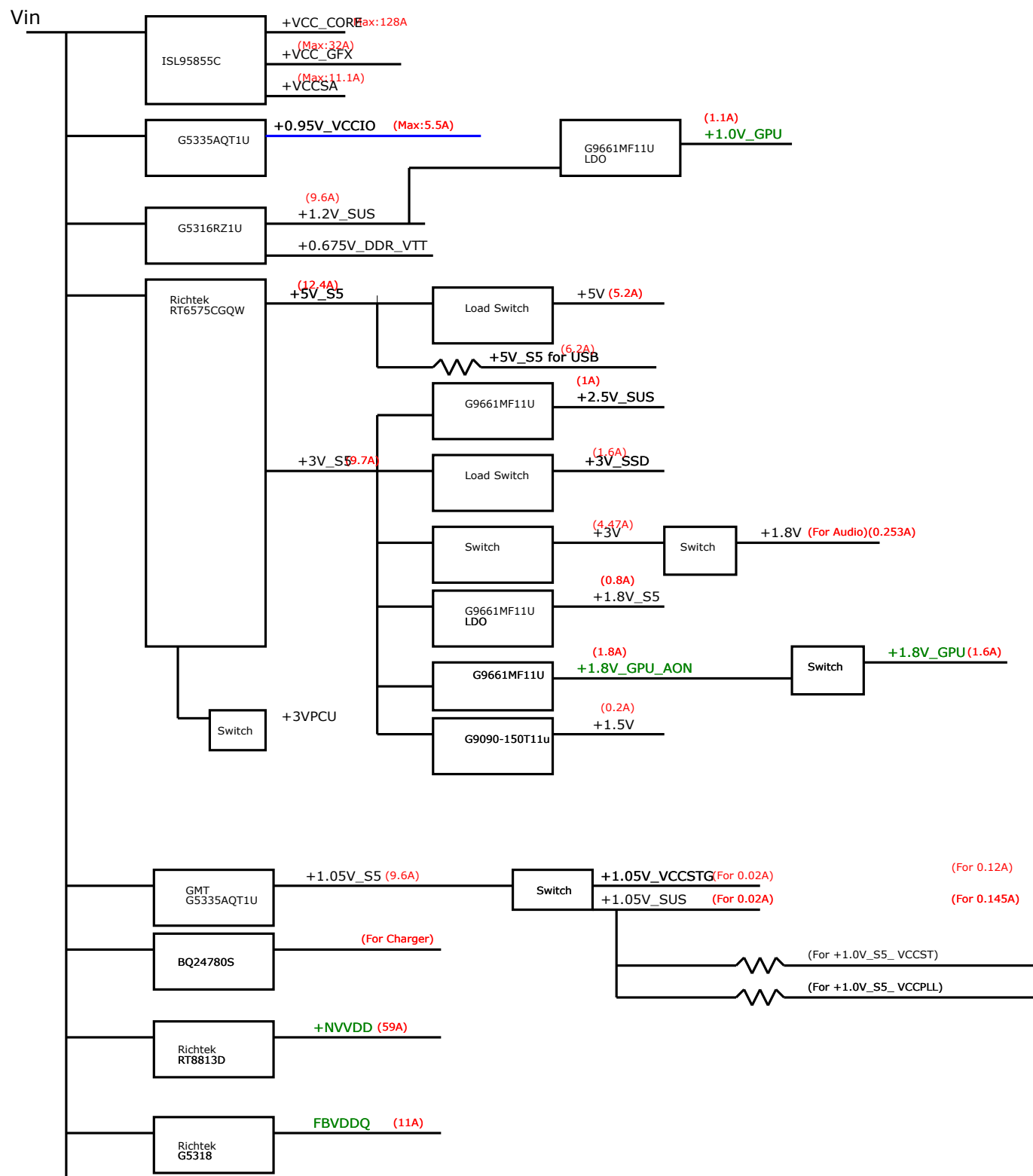
< 20ms

Discharge



OVR-M(N18P-G61/G62)







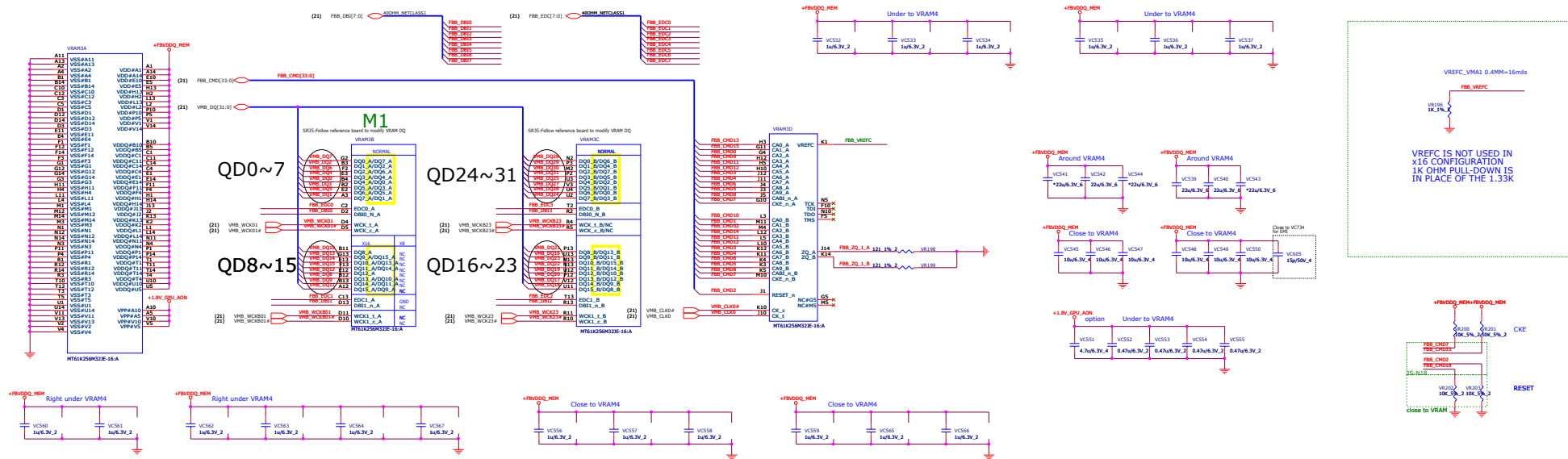


OS status	S0	S0ix	S3	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	
H/W status	S0	C10	S3	S4 (Win10 off) RTC wake Enable WOLAN Enable	S4 (Win10 off) RTC wake Disable WOLAN Disable	S5 (Fast Startup "y")	S5 (Fast Startup "x")	
RUN_ON	H	H	L	L	L	L	L	
+3V	H	H	L	L	L	L	L	
+5V	H	H	L	L	L	L	L	
+0.675V_DDR_VTT	H	H	L	L	L	L	L	
+VCCSA	H	H	L	L	L	L	L	
+VCC_GFX	H	H	L	L	L	L	L	
+VCC_CORE	H	H	L	L	L	L	L	
C10_GATE	H	L	L	L	L	L	L	
+1.05V_VCCSTG	H	L	L	L	L	L	L	
+0.95V_VCCIO	H	L	L	L	L	L	L	
+1.2V_SUS_C10(VCCPLL_OC)	H	L	L	L	L	L	L	
SUS_ON	H	H	H	L	L	L	L	
+1.05V_VCCPLL/+1.05V_VCCST	H	H	H	L	L	L	L	
+1.05V_SUS	H	H	H	L	L	L	L	
+1.2V_SUS	H	H	H	L	L	L	L	
SUS_ON_2.5V	H	H	H	L	L	L	L	
+2.5V_SUS	H	H	H	L	L	L	L	
S5_ON_2	H	H		H	L	L	L	
+1.05V_S5	H	H		H	L	L	L	
S5_ON	H	H		H	L	H	L	
+3V_S5	H	H		H	L	L	L	
+1.8V_S5(From PCH)	H	H		H	L	H	L	
+5V_S5	H	H		H	L	H	L	



Quanta Computer Inc.
PROJECT : FX506L/FX706L

MEMORY: FBB Partition 31..0



MEMORY: FBB Partition 63..32

